Computer-Based Instruments

NI 5411/5431 User Manual

PXI™/PCI/ISA High-Speed Arbitrary Waveform Generator
PXI/PCI Video Waveform Generator

NATIONAL INSTRUMENTS™

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Conventions

The following conventions are used in this manual:

<>	Angle brackets that contain numbers separated by an ellipsis represent a range of values associated with a bit or signal name—for example, DBIO<3..0>.
»	The » symbol leads you through nested menu items and dialog box options to a final action. The sequence **File»Page Setup»Options** directs you to pull down the **File** menu, select the **Page Setup** item, and select **Options** from the last dialog box.
♦	The ♦ symbol indicates that the following text applies only to a specific product, a specific operating system, or a specific software version.
	This icon denotes a note, which alerts you to important information.
	This icon denotes a caution, which advises you of precautions to take to avoid injury, data loss, or a system crash.
bold	Bold text denotes items that you must select or click on in the software, such as menu items and dialog box options. Bold text also denotes parameter names.
italic	Italic text denotes variables, emphasis, a cross reference, or an introduction to a key concept.
`monospace`	Text in this font denotes text or characters that you should enter from the keyboard. This font is also used for the proper names of functions, variables, and filenames and extensions.
`monospace italic`	Italic text in this font denotes text that is a placeholder for a word or value that you must supply.
NI 5411/5431	Refers to the NI 5411 and the NI 5431, unless otherwise noted.

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Generating Waveforms with the NI 5411/5431

The *NI 5411/5431 User Manual* describes the features, functions, and operation of the NI 5411 arbitrary waveform generator and the NI 5431 arbitrary video generator. These high-speed devices perform comparably to standalone instruments while providing the flexibility of computer-based operation.

About Your NI 5411/5431

Thank you for buying a National Instruments NI 5411 arbitrary waveform generator or NI 5431 arbitrary video generator. The NI 5411 family consists of three different devices:

- NI 5411 for ISA
- NI 5411 for PCI
- NI 5411 for PXI

The NI 5431 family consists of two different devices:

- NI 5431 for PCI
- NI 5431 for PXI

Your NI 5411/5431 device has the following features:

- One 12-bit resolution output channel
- Up to 16 MHz sine and transistor-transistor logic (TTL) waveform output for the NI 5411
- Up to 8 MHz sine and TTL waveform outputs for the NI 5431
- Software-selectable output impedances of 50 Ω and 75 Ω
- Output attenuation levels from 0 to 73 dB
- Phase-locked loop (PLL) synchronization to external clocks
- Sampling rate up to 40 MS/s
- Up to 8,000,000-sample onboard waveform memory
- Waveform linking and looping for arbitrary waveform generation
- Digital and analog filters
- 32-bit direct digital synthesis (DDS) for standard function generation
- External trigger input
- Marker as trigger output
- 16-bit digital pattern generation with clock
- Real-Time System Integration (RTSI) and PXI triggers

All NI 5411 devices follow industry-standard Plug and Play specifications on both buses and offer seamless integration with compliant systems. If your application requires more than one channel of arbitrary waveform generation, you can synchronize multiple devices on all platforms using RTSI/PXI bus triggers on devices that use the RTSI/PXI bus or the digital trigger on the I/O connector.

Detailed specifications for the NI 5411/5431 devices are in Appendix A, *Specifications*.

Connecting Signals

Figure 1-1 shows the front panels for the NI 5411/5431 for the PXI, PCI, and ISA buses. The front panel contains three types of connectors: BNC, SMB, and 50-pin very high-density SCSI (VHDSCSI). The main waveform is generated through the connector labeled ARB for the NI 5411 and Video Out for the NI 5431.

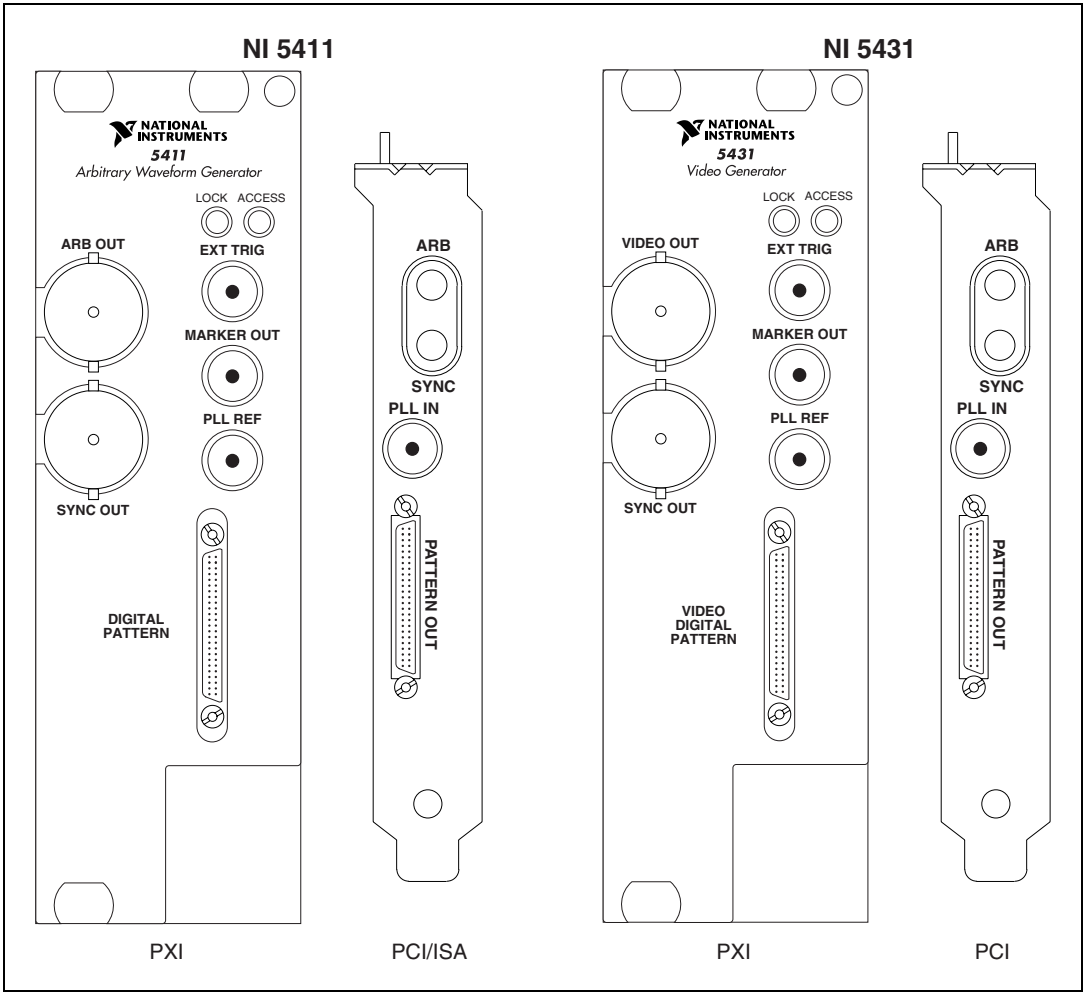

Figure 1-1. NI 5411/5431 I/O Connectors

ARB/ Video Out Connector

The ARB/Video Out connector provides the waveform output. The maximum output levels on this connector depend on the type of load termination. If the output of your NI 5411/5431 terminates into a 50 Ω load, the output levels are ±5 V, as shown in Figure 1-2. If the output of your NI 5411/5431 terminates into a high-impedance load (HiZ), the output

levels are ±10 V. If the output terminates into any other load, the levels are as follows:

$$V_{out} = \pm\frac{R_L}{R_L + R_O} \times 10\ \text{V}$$

where V_{out} is the maximum output voltage level
R_L is the load impedance in ohms, and
R_O is the output impedance on the NI 5411/5431.

By default, R_O = 50 Ω, but you can use your software to set it to 75 Ω.

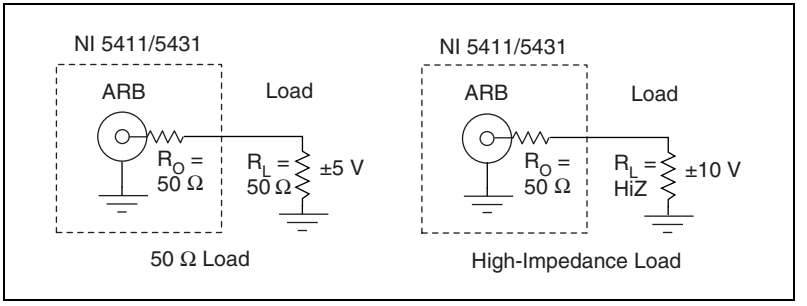

Figure 1-2. Output Levels and Load Termination Using a 50 Ω Output Impedance

Note Software sets the voltage output levels based on a 50 Ω load termination. If you are using the NI 5431, you should use your software to select R_O = 75 Ω for video generation.

For more information on waveform generation and analog output operation, refer to Chapter 2, *Arb Operation*. For specifications on the waveform output signal, see Appendix A, *Specifications*.

- NI 5431

Caution Do not set the output voltage level for your NI 5431 to more than ±1 V into 75 Ω, as this may damage your video display device or your device under test (DUT). Always check the output levels before connecting a DUT to your NI 5431. National Instruments is not responsible for any damage caused to your DUT.

SYNC Connector

The SYNC connector provides a TTL version of the sine waveform being generated at the output. You can think of the SYNC output as a very high-frequency resolution, software-programmable clock source for many applications. You can also vary the duty cycle of the SYNC output on the fly by software control, as shown in Figure 1-3. t_p is the time period of the sine wave being generated and t_w is the pulse width of the SYNC output. The duty cycle is $(t_w/t_p) \times 100\%$.

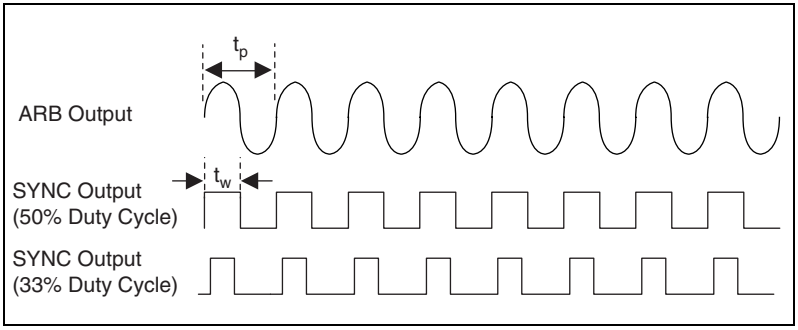

Figure 1-3. SYNC Output and Duty Cycle

You can route the SYNC output to the RTSI lines over the RTSI bus for your NI 5411/5431 for PCI and NI 5411 for ISA. You can also route the SYNC output to the TTL trigger lines over the TTL trigger bus for your NI 5411/5431 for PXI. The SYNC output is derived from a comparator connected to the analog waveform and provides a meaningful waveform only when you are generating a sine wave on the ARB output. For more information on SYNC output, see Chapter 2, *Arb Operation*.

PLL Ref/External Clock Connector

The PLL Ref/External Clock connector on your NI 5411/5431 has different uses depending on which NI 5411/5431 device you are using. These different applications are described in the following sections.

- NI 5411

The PLL Ref connector is a phase-locked loop (PLL) input connector that can accept a reference clock from an external source and phase lock the NI 5411 internal clock to this external clock. The reference clock should not deviate more than ±100 ppm from its nominal frequency. The minimum amplitude levels of 1 $V_{pk\text{-}pk}$ are required on this clock. You can lock reference clock frequencies of 1 MHz and 5–20 MHz in 1 MHz steps.

Note You can phase lock the NI 5411 for PCI/ISA to other National Instruments devices over the RTSI bus using the 20 MHz RTSI clock signal. You can phase lock the NI 5411 for PXI to other National Instruments devices using the 10 MHz backplane clock.

If no external reference clock is available, the NI 5411 automatically tunes the internal clock to the highest accuracy possible. For more information on PLL operation, refer to Chapter 2, *Arb Operation*.

- NI 5431

  Do not use this connector for phase locking to an external source. It is reserved for future use and other functionality.

- NI 5411/5431 for PXI

  In addition to phase locking (on the NI 5411), this connector is also used to provide input from an external update clock. You can select this functionality on your NI 5411/5431 through your software. You can feed a TTL/CMOS-level clock to this connector with a maximum frequency of 40 MHz.

Note You must *not* change the external clock while waveform generation is in progress. Only modify the frequency of the external clock before you start the waveform generation or after you stop the waveform generation.

Dig Out Connector

Dig Out is a 16-bit digital I/O connector that contains the 16-bit digital pattern outputs, digital pattern clock output, marker output, external trigger input, and +5 V power output.

Connector Pin Assignments

Figure 1-4 shows the NI 5411/5431 50-pin digital connector. Refer to Table 1-1 for a description of the signals.

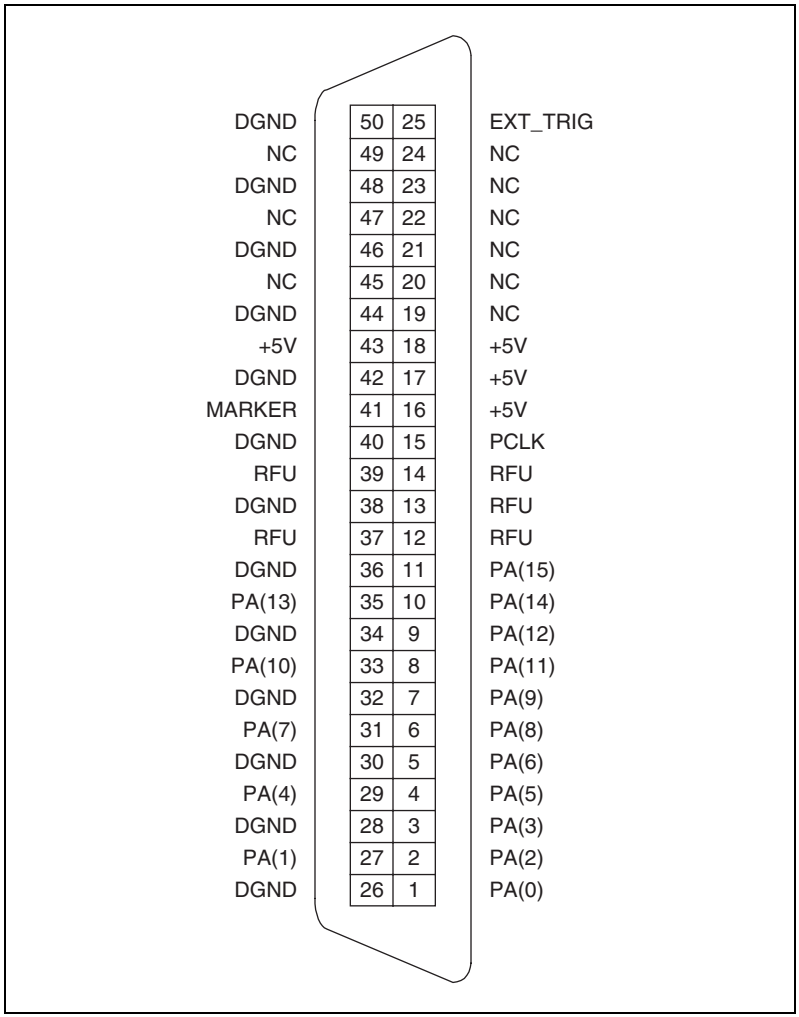

Figure 1-4. NI 5411/5431 50-Pin Digital Output Connector Pin Assignments

Signal Descriptions

Table 1-1 shows the pin names and signal descriptions used on the NI 5411/5431 digital output connector.

Table 1-1. Digital Output Connector Signal Descriptions

Signal Name	Type	Description
DGND	—	Digital ground
EXT_TRIG	Input	External trigger—The external trigger input signal is a TTL-level signal that you can use to start or step through a waveform generation. For more information on trigger sources and trigger mode, see Chapter 2, *Arb Operation*.
MARKER	Output	Marker—A marker is a TTL-level output signal that you can set up at any point in the waveform being generated. You can use this signal to synchronize or trigger other devices at a certain time within waveform generation.
NC	—	Not connected.
PA<0..15>	Output	Digital pattern outputs—The 16-bit digital representation of the analog waveform is available on these output pins as digital pattern outputs along with the PCLK signal to which it is synchronized. This data is available directly from the memory after some sample clocks pipeline delay. The digital pattern outputs are TTL output levels.
PCLK	Output	Digital pattern clock—The digital pattern clock output synchronizes the digital pattern output. This data is available directly from the memory after some sample clocks pipeline delay. The PCLK output is a TTL output level.
RFU	—	Reserved for future use. Do not connect signals to this pin.
+5V	Output	+5 V power—A +5 V output signal is available on the NI 5411/5431 to power external devices. The maximum current you can draw is 100 mA.

SHC50-68 50-Pin Cable Connector

You can use an optional SHC50-68 50-pin to 68-pin cable for pattern generation output. The cable connects to the digital output connector on the NI 5411/5431. Figure 1-5 shows the 68-pin connector pin assignments on the SHC50-68 cable.

Note The SHC50-68 connector uses the same signals as the NI 5411/5431 digital output connector shown in Table 1-1.

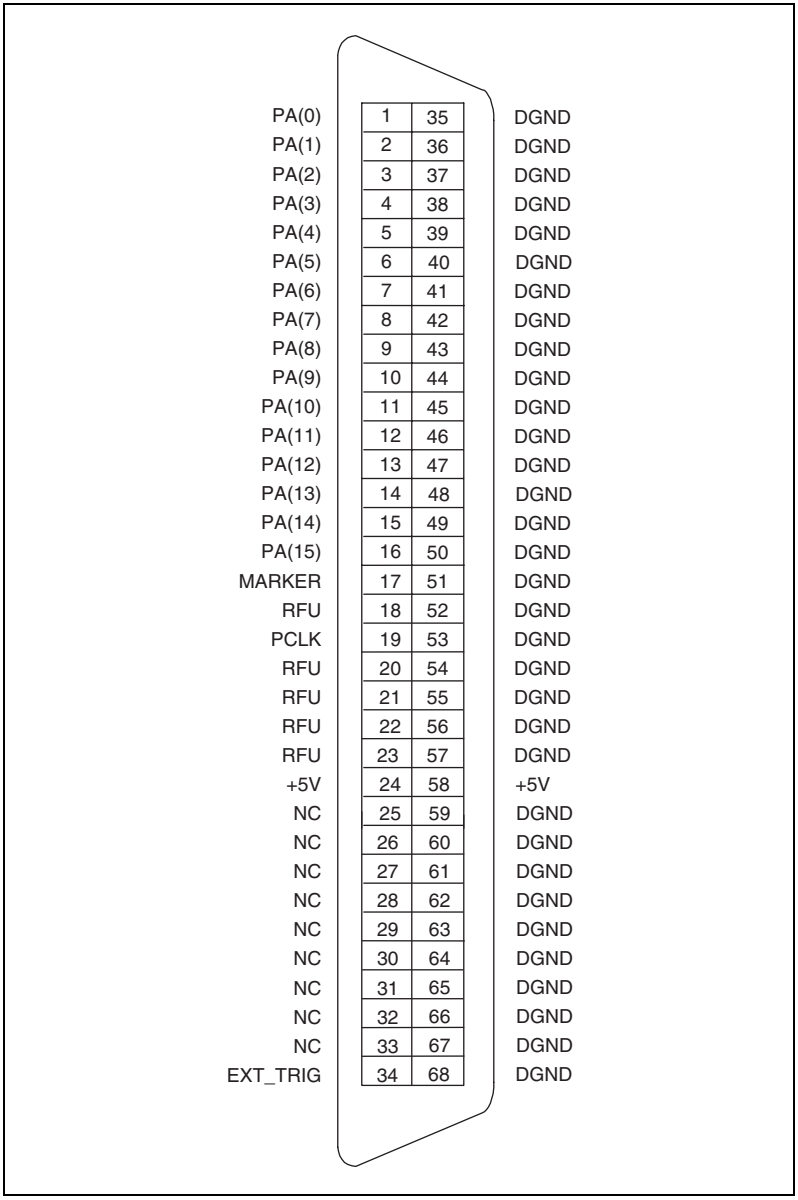

Figure 1-5. SHC50-68 68-Pin Connector Pin Assignments

Software Options for Your NI 5411/5431

This section describes the NI-FGEN driver software and development tools that you can use to create application software for your NI 5411/5431.

Software Included with Your NI 5411/5431

Your NI 5411/5431 kit includes several VirtualBench *soft front panels* to help you get up and running quickly with your waveform generator. These soft front panels are an onscreen interface similar to standalone instruments. An NI-FGEN instrument driver is also included, which you can use with a wide variety of development tools to build applications for your NI 5411/5431.

These software tools are discussed in the following sections.

VirtualBench

Similar to standalone instruments, VirtualBench acquires, controls, analyzes, and presents data. However, since VirtualBench operates on your PC, it provides additional processing, storage, and display capabilities.

VirtualBench loads and saves waveform data in a form that popular spreadsheet programs and word processors can use. It can also generate reports—a complement to the raw data storage—by adding timestamps, measurements, user names, and comments. You can print the waveforms and the settings of VirtualBench to a printer connected to the PC.

VirtualBench has three components—VirtualBench-FG, Waveform Editor, and VirtualBench-Arb—that you can use with your NI 5411/5431. These components are described in the following sections.

VirtualBench-FG

VirtualBench-FG transforms your PC into a fully featured function generator that rivals desktop models by using the DDS capabilities of your NI 5411/5431. VirtualBench-FG emulates benchtop function generators, so you can quickly learn to use computer-based instruments.

With VirtualBench-FG, you can generate a variety of waveforms, including five standard waveforms: sine, square, triangle, rising exponential, and falling exponential. Using VirtualBench-FG, you load waveforms from an ASCII text file and generate them repeatedly. You can generate these waveforms with a resolution of approximately 10 mHz and perform

frequency sweeps and shift-keying. As with all VirtualBench instruments, you can load and save instrument settings.

Waveform Editor

You use the Waveform Editor to create, sketch, and edit complex waveforms that the VirtualBench-Arb player can then generate. A library of standard waveforms for creating complex waveforms is included, and you can also write equations to create arbitrary waveforms and view the waveforms in a time or frequency domain.

VirtualBench-Arb

VirtualBench-Arb uses the arbitrary waveform generation capabilities of your NI 5411/5431 to generate a wide variety of signals. You can use VirtualBench-Arb to configure your NI 5411/5431 and to download waveforms created in the Waveform Editor. The VirtualBench-Arb **Sequence Editor** allows you to create complex arbitrary waveforms by using the linking and looping features of your NI 5411/5431.

NI-FGEN Instrument Driver

To create your application, you need an industry-standard software driver such as NI-FGEN to control your instrument. The NI-FGEN driver includes a set of standard functions for configuring, creating, starting, and stopping waveform generation. The instrument driver reduces your program development time and simplifies instrument control by eliminating the need to learn a complex programming protocol for your instrument.

NI-FGEN is in a standard instrument driver format that works with LabVIEW, LabWindows/CVI, and conventional programming languages such as C, C++, and Visual Basic.

Refer to the NI-FGEN `readme.txt` file for more details on the NI-FGEN instrument driver. This file can be launched from the **Start»Programs»National Instruments FGEN** menu.

Note An *NI-FGEN Instrument Driver Quick Reference Guide* is included in your NI 5411/5431 kit. This reference guide helps you program your NI 5411/5431.

Additional National Instruments Development Tools

The following sections describe several additional tools that you can use to develop complex applications for your NI 5411/5431. The NI-FGEN instrument driver exposes the Application Programming Interfaces (APIs) to these development environments.

LabVIEW

LabVIEW is a graphical programming language for building instrumentation systems. With LabVIEW, you quickly create front panel user interfaces, giving you interactive control of your software system. To specify the functionality, you assemble block diagrams—a natural design notation for engineers and scientists. LabVIEW has all of the same development tools and language capabilities of a standard language such as C, including looping and case structures, configuration management tools, and compiled performance.

Note Use the NI-FGEN instrument driver to program and control your NI 5411/5431 using LabVIEW.

LabWindows/CVI

LabWindows/CVI is an interactive, ANSI C programming environment designed for automated test applications.

LabWindows/CVI has an interactive drag-and-drop editor for building your user interface and a complete ANSI C development environment for building your test program logic. The LabWindows/CVI environment has a wide collection of automatic code-generation tools and utilities that accelerate your development process, without sacrificing any of the power and flexibility of a language such as C. In addition, the LabWindows/CVI run-time libraries are compatible with standard C/C++ compilers, including Visual C++ and Borland C++ under Windows.

Note Use the NI-FGEN instrument driver to program and control your NI 5411/5431 using LabWindows/CVI.

ComponentWorks

ComponentWorks is a collection of 32-bit ActiveX controls for building virtual instrumentation systems. ComponentWorks gives you the power and flexibility of standard development tools, such as Microsoft Visual Basic or Visual C++, with the instrumentation expertise of National Instruments. Based on ActiveX technology, ComponentWorks controls are

easy to configure using property sheets and are easy to control from your programs using high-level properties and methods. ComponentWorks features instrumentation-based graphical user interface (GUI) tools, including graphs, meters, gauges, knobs, dials, and switches.

Note Use the NI-FGEN instrument driver to program and control your NI 5411/5431 using ComponentWorks.

Using the Soft Front Panels to Generate Waveforms

You use the VirtualBench soft front panels to interactively control your NI 5411/5431 as you would a desktop function generator or an arbitrary waveform generator.

Generating Standard Functions

If you need to generate standard waveforms such as a sine, square, ramp, or DC signal, you can use the VirtualBench-FG soft front panel shown in Figure 1-6. Launch the front panel by selecting **Start»Programs»National Instruments FGEN»VirtualBench FG**. You use this front panel to control the frequency, amplitude, offset, and type of waveform generated. For the NI 5411, the maximum sine frequency you can generate is 16 MHz. For the NI 5431, the maximum frequency is limited to 8 MHz. The maximum amplitude is 5 V_{pk} into a 50 Ω load. If the load is a high-impedance load, the actual levels will be twice that shown on the front panel.

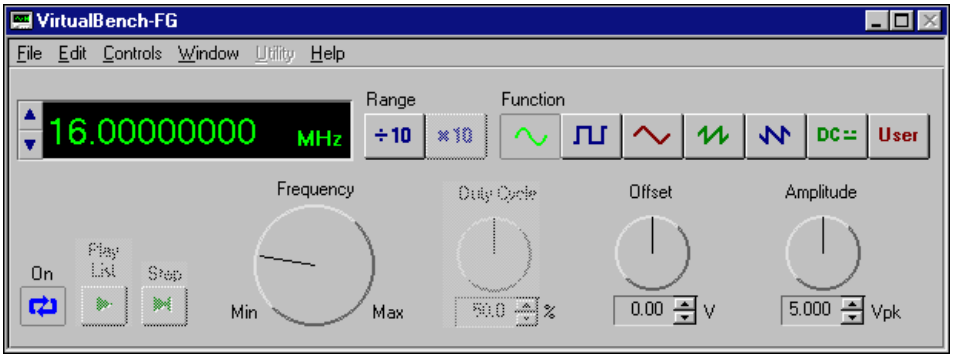

Figure 1-6. VirtualBench-FG Soft Front Panel for Function Generation

To control additional instrument parameters, select **Edit»54xx Settings** to bring up the dialog box shown in Figures 1-7 and 1-8.

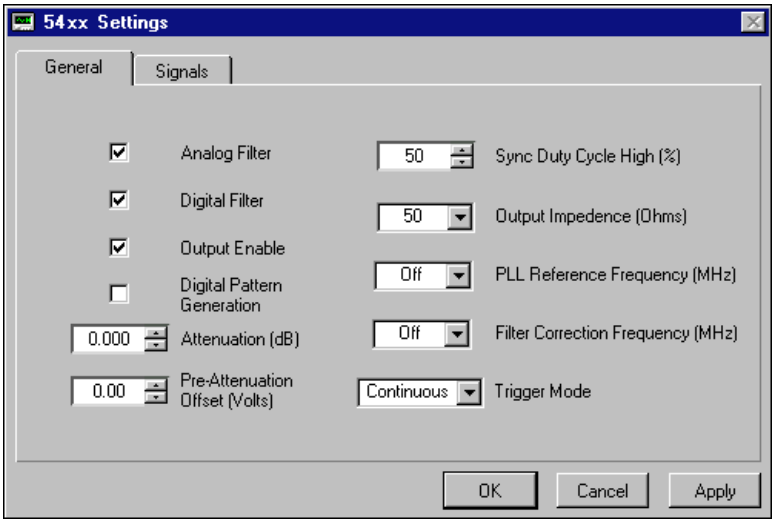

Figure 1-7. VirtualBench-FG General Settings Dialog Box for the NI 5411

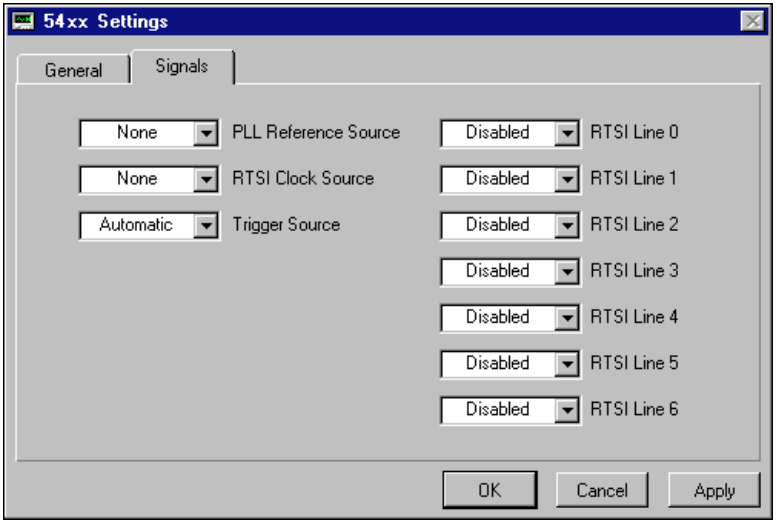

Figure 1-8. VirtualBench-FG Signals Settings Dialog Box for the NI 5411

Note Refer to the online help for further information about the **54xx Settings** dialog box.

You can also load a custom waveform pattern with VirtualBench-FG. This waveform should be a text file and should contain exactly 16,384 samples. If the defined waveform does not contain exactly 16,384 samples, you may see undesired effects in your waveform output. Follow these steps to load a custom waveform:

1. Select **File»Load Waveform** to bring up the dialog box shown in Figure 1-9.

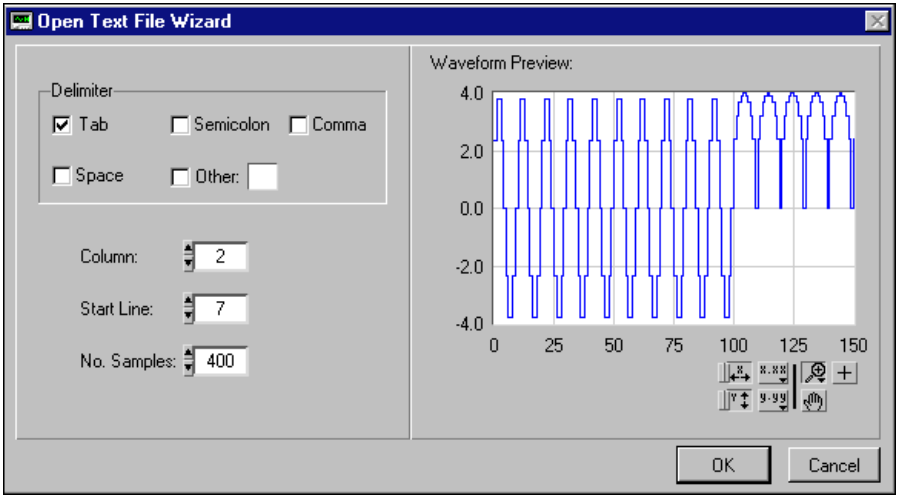

Figure 1-9. VirtualBench-FG Load Waveform Dialog Box

2. Specify the delimiter used in the text file, the number of columns, the start line, and the number of samples.
3. Click **OK** to return to the main VirtualBench-FG screen shown in Figure 1-6.
4. Click the **User** button to use the information in the text file as the source for the waveform.
5. Click the **On** button to generate the waveform.

Generating Multiple Frequencies in a Sequence

If desired, you can generate multiple frequencies in a sequence, which can include frequency sweeping, hopping, and so on. You can list up to 512 different frequencies and specify the duration of generation for each of

them using the VirtualBench-FG Frequency List Editor. Follow these steps to create a list of multiple frequencies:

1. Select **Window»Frequency List Editor** from the VirtualBench-FG soft front panel to bring up the dialog box shown in Figure 1-10.

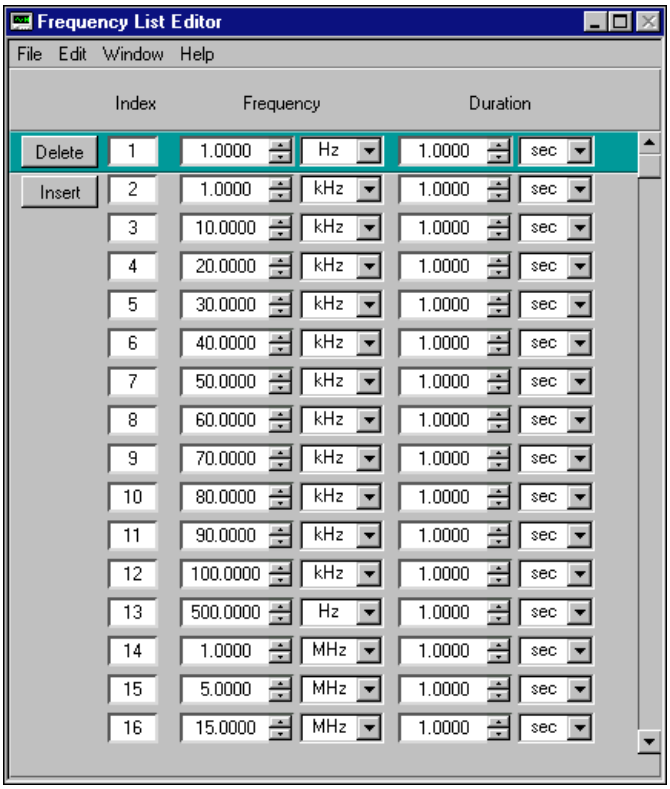

Figure 1-10. VirtualBench-FG Frequency List Editor Dialog Box

2. Specify the frequency and duration of each function in the sequence.
3. Save the sequence by selecting **File»Save**.
4. To return to the main VirtualBench-FG screen shown in Figure 1-6, select **File»Close**.
5. Select **File»Load Frequency List** to load the frequency list.

You can combine the frequency list generation with different trigger modes to get the desired frequency generation.

Arbitrary Waveform Generation

The NI 5411 and NI 5431 are full-featured arbitrary waveform generators that you can use to create and generate any arbitrary waveform up to a sample rate of 40 MHz. The soft front panels described in the following sections help you create and generate complex arbitrary waveforms.

Waveform Editor

You can use the Waveform Editor shown in Figure 1-11 to create a custom waveform. To launch the Waveform Editor, select **Start»Programs» National Instruments FGEN»Waveform Editor**. You can select waveforms from the function library, write equations, or draw them manually. Each segment can have more than one waveform component in it, and you can perform a variety of math functions on each component.

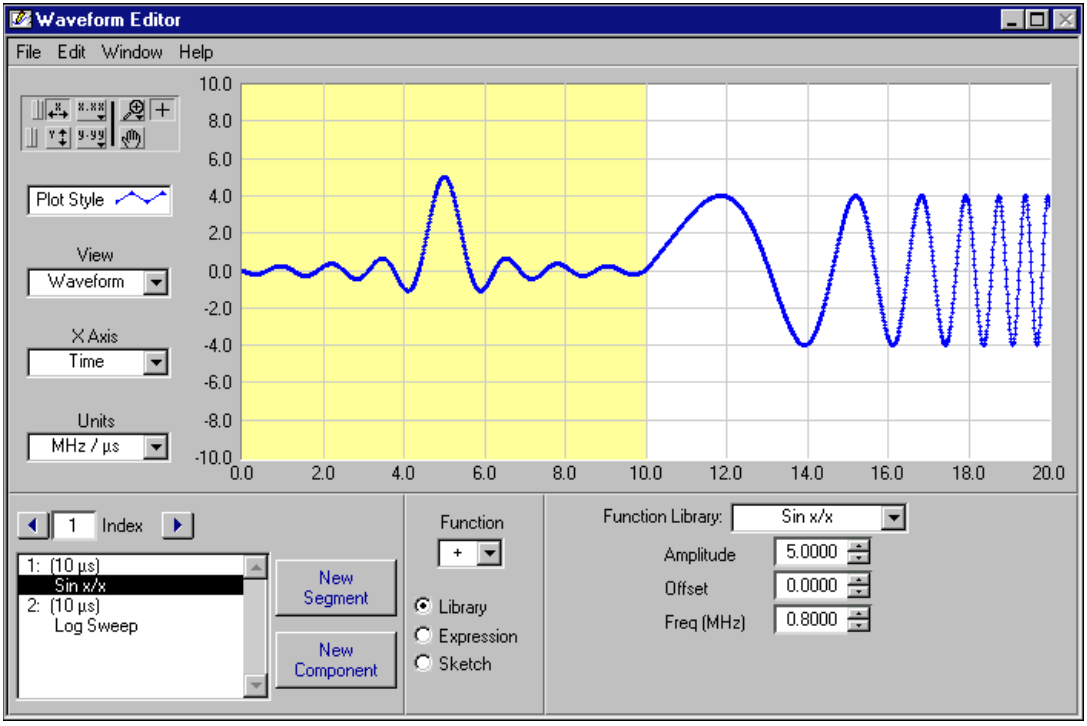

Figure 1-11. Waveform Editor Soft Front Panel

This soft front panel is resizable so you can view the waveforms you create with as much precision as you wish. You can save the waveforms in the following formats:

- Voltage (`.wfm`)
- Text (`.txt`)
- Binary (`.bin`)

Binary waveforms are the preferred format for the NI 5411/5431. This format is the fastest to calculate and download, and creates the smallest size file.

Waveform Player

After you have created your custom waveform, you can generate the waveform using a waveform player, such as VirtualBench-Arb, which is shown in Figure 1-12. Launch VirtualBench-Arb by selecting **Start»Programs»National Instruments FGEN»VirtualBench Arb**. With VirtualBench-Arb, you can specify the update rate for the waveform and download and play voltage (`.wfm`), text (`.txt`), or binary (`.bin`) waveforms.

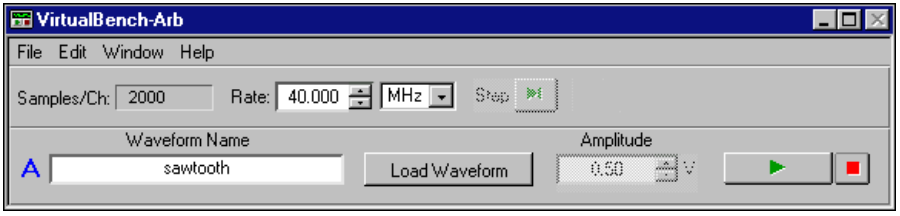

Figure 1-12. VirtualBench-Arb Soft Front Panel

Note The NI 5411/5431 must have at least 256 samples in the waveform, and the buffer size should be a multiple of 8 samples.

Linking, Looping, and Markers Using the Sequence Editor

All the waveforms created using the Waveform Editor are single buffer waveforms stored as a file. The NI 5411/5431 has features such as linking and looping that you use to load multiple buffers in the instrument. After buffers have been loaded in the instrument, you can address them in any sequence by using the Sequence Editor shown in Figure 1-13. To launch the Sequence Editor, select **Window»Sequence Editor** from the VirtualBench-Arb soft front panel.

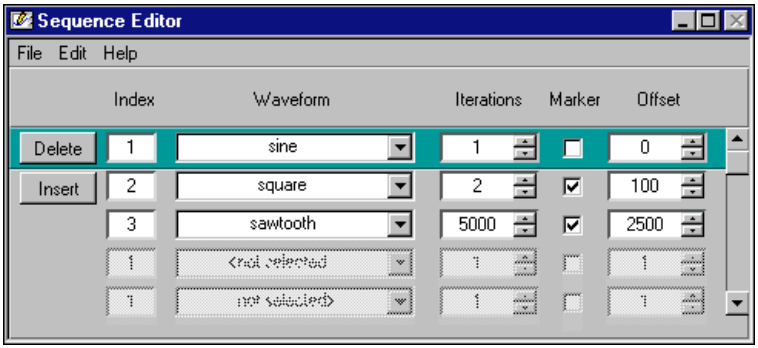

Figure 1-13. VirtualBench-Arb Sequence Editor Dialog Box

To use the linking and looping features, perform the following steps:

1. Save the files in binary format and put them in the same folder.
2. Select **Edit»Project Folders**.
3. Delete any folders which are shown in the window.
4. Click the **Add** button and select the folders where the your binary files are stored. All of the binary files in the specified project folders appear as selections under the **Waveform** column.

Note All the binary files from the selected project folders are loaded in the instrument, whether you use the files for generation or not. So, you should create project folders with only the desired waveform binary files to avoid long download times and "memory full" errors.

5. Click **OK** to return to the Sequence Editor.
6. In the Sequence Editor, select the iterations and a marker location for each of up to 290 binary waveforms.
7. Save this sequence as a *filename*.seq file by selecting **File»Save**.
8. In the VirtualBench-Arb main soft front panel, click the **Load Waveform** button and load the *filename*.seq file.

The sequence of these waveforms appears as the output.

You can combine the sequences, trigger modes, and software trigger (Step) to generate the desired waveforms.

Power-Up and Reset Conditions

When you power up your computer, the NI 5411/5431 is in the following state:

- The output is disabled and set to 0 V.
- The sample clock is set to 40 MHz.
- The trigger mode is set to continuous.
- The trigger source is set to automatic (the software provides the triggers).
- The digital filter is enabled.
- Digital pattern generation is disabled.
- Output attenuation remains unchanged from its previous setting.
- The analog filter remains unchanged from its previous setting.
- Output impedance remains unchanged from its previous setting.

When you reset the board using NI-FGEN or any other application software, your NI 5411/5431 is in the same state as shown at power up, previously listed, with the following differences:

- Output attenuation is set to 0 dB.
- The analog filter is enabled.
- Output impedance is set to 50 Ω.
- The PLL reference frequency is set to 20 MHz (NI 5411 only).
- The PLL reference source is set to internal tuning (NI 5411 only).
- The RTSI clock source is disabled (NI 5411 for PCI only).
- The SYNC duty cycle is set to 50%.

2

Arb Operation

This chapter describes how to use your NI 5411/5431.

Figure 2-1 shows the NI 5411/5431 block diagram.

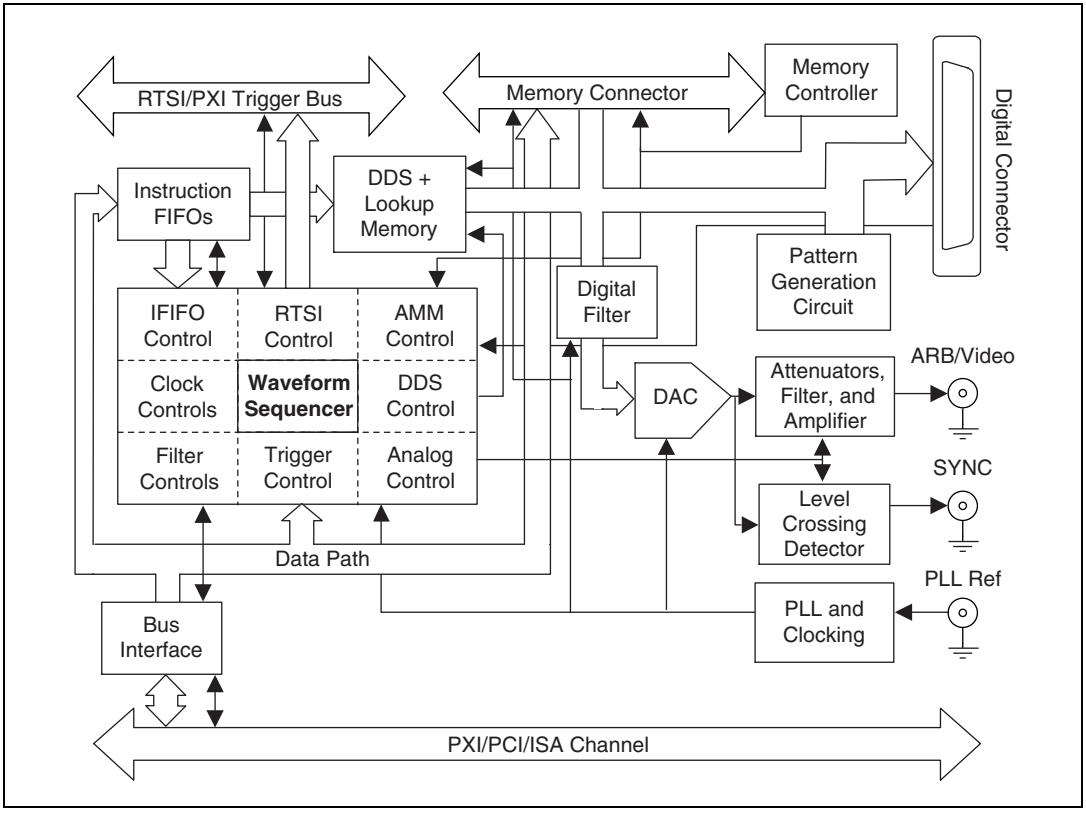

Figure 2-1. NI 5411/5431 Block Diagram

The NI 5411/5431 has several main components:

- A PXI, PCI, or ISA bus interface that handles Plug and Play protocols for assigning resources to the device and providing drivers for the data and address bus that are local to the device
- A waveform sequencer that performs multiple functions such as arbitrating the data buses and controlling the triggers, filters, attenuators, clocks, PLL, RTSI switch, instruction FIFO, and DDS
- A memory controller that controls the waveform memory on the memory module. The data from the memory is fed to a digital-to-analog converter (DAC) through a half-band interpolating digital filter. The output from the DAC goes through the filter to the amplifiers, attenuators, and, finally, the I/O connector.

Generating Waveforms

The NI 5411/5431 generates waveforms in two modes: Arb and DDS. Use Arb mode for any arbitrary waveform generation, and use DDS mode for standard frequency generation such as sine, TTL, square, and triangular waveforms.

Arb mode, which has more features and is more flexible than DDS mode, allows you to define waveforms as multiple buffers. You can then link and loop these buffers in any order you want.

Note If you use VirtualBench software, you must use VirtualBench-Arb for Arb mode.

DDS mode is better for generating standard waveforms that are repetitive in nature, such as sine, TTL, square, and triangular waveforms. DDS mode limits you to one buffer, and the buffer size must be exactly equal to 16,384 samples.

Note If you use VirtualBench software, you must use VirtualBench-FG for DDS mode.

Figure 2-2 shows a block diagram of the data path for waveform generation. The data for waveform generation can come from either the waveform memory module or DDS lookup memory, depending on the mode of waveform generation. This data is interpolated by a half-band digital filter and then fed to a high-speed DAC. The data has a pipeline delay of 26 update clocks through this digital filter. Although the digital filter can be disabled through software, there will still be a 26 update clock delay.

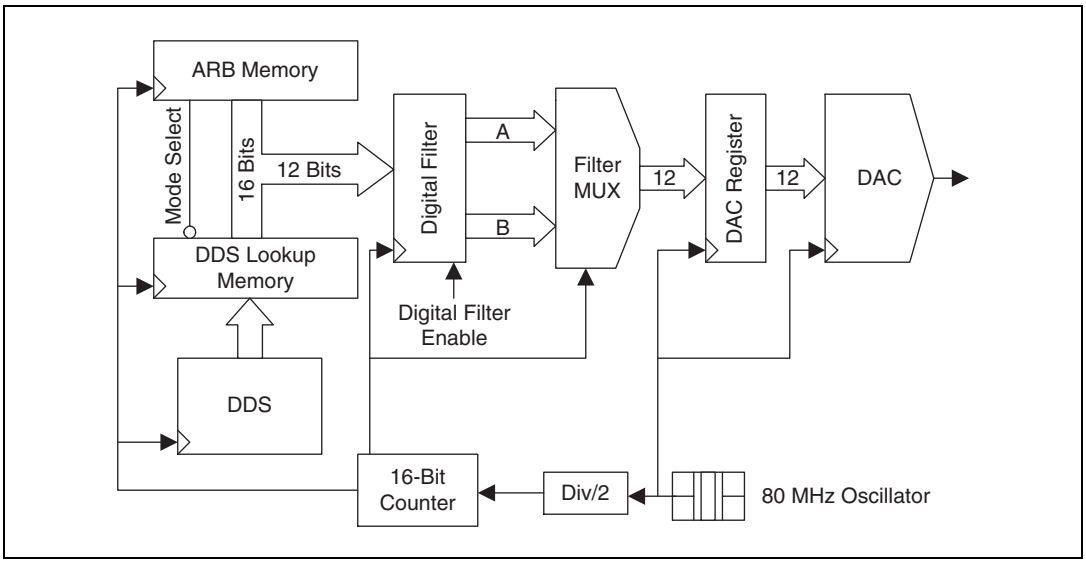

Figure 2-2. Waveform Data Path Block Diagram

On the NI 5411/5431, the high-speed DAC is always updated at 80 MHz, but the maximum update clock for waveform memory is 40 MHz. The update clock for the waveform memory can be further divided by a 16-bit counter, as shown in Figure 2-2. Therefore, the slowest update rate is 40 MHz divided by 65,536, which is 610.35 Hz.

Note For DDS mode, you should always keep the update rate at 40 MHz.

- NI 5431

  To achieve a maximum update rate of exactly 40 MHz, you must set the **Video Waveform Type** to PAL with your software. If the setting is NTSC, the maximum update rate will not be exactly 40 MHz.

- NI 5411/5431 for PXI

  You may use an external clock source as the update clock. To avoid board problems, do not change the frequency of this clock during waveform generation. Change the frequency only before initiating the waveform generation. If any malfunction occurs, stop the waveform generation and reset the board to a known state before restarting.

These boards also support an internal high-resolution clocking mode. When you use this type of clock, you can set the update clock frequency to any value from 0 to 40 MHz with a resolution of approximately 40 mHz. This mode is useful for applications that require a precise clock source, which is impossible with the default counter-based clocking scheme.

Note For the NI 5431 for PXI, you must set the **Video Waveform Type** setting to PAL with your software before using the high-resolution clocking mode.

Arb Mode

The Arb mode of waveform generation uses a separate *waveform memory* for storing multiple waveform buffers. This mode also uses a FIFO memory for storing the *staging list*, which contains the buffer linking and looping information. This FIFO is referred to as an *instruction FIFO*.

Waveform Size and Resolution

The NI 5411/5431 stores arbitrary waveforms in memory as 16-bit digital words. Only the 12 most significant bits are sent to the digital filter and the DAC. The following sections describe the waveform memory, the sizes available, and minimum buffer size.

Waveform Memory

The NI 5411/5431 uses a waveform memory that is 16 bits wide. The standard memory size for the NI 5411 is 2,000,000 samples, and for the NI 5431 is 8,000,000 samples. With a minimum standard memory size of 2,000,000 samples, you can store very long waveforms on the board and obtain reliable waveform generation even at full speed. You can upgrade the NI 5411 to an 8,000,000-sample waveform memory by installing the 16 MB memory module. See Appendix B, *Optional Accessories*, for more information on the installation of the optional memory module.

As shown in Figure 2-3, a 2,000,000-sample waveform memory is organized as eight banks of 256 k by 16-bit memory chips. An 8,000,000-sample waveform memory is organized as eight banks of 1 M by 16-bit memory chips. These eight banks are then shifted serially to achieve a single data stream of 16-bit words at 40 MHz.

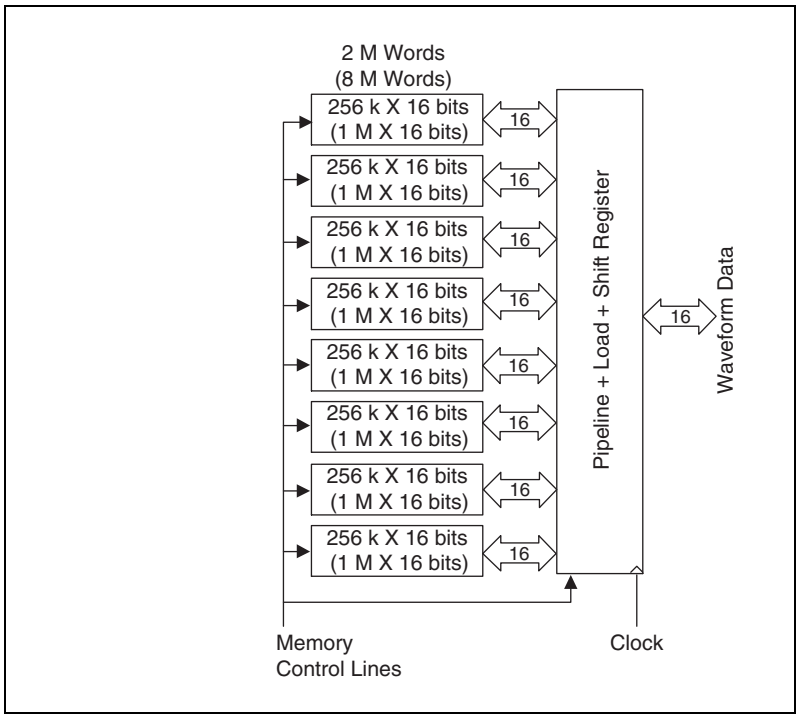

Figure 2-3. Waveform Memory Architecture

Minimum Buffer Size and Resolution

The NI 5411/5431 device memory architecture imposes certain restrictions on the buffer size and resolution. The minimum buffer size for Arb mode is 256 samples, and the buffers must be in multiples of eight samples. If these buffer requirements are not met, NI-FGEN returns an error. For example, if you request the NI 5411/5431 to load a buffer of 257 samples, NI-FGEN will return an error.

Before you begin generating waveforms, you must load the buffers on your NI 5411/5431. Each signal to be generated is loaded into the memory in the form of 16-bit digital samples. A finite number of these samples makes a *waveform buffer*, also called a *waveform segment*. You can load multiple buffers in the memory of the NI 5411/5431. To generate these buffers, you prepare a *staging list*, or a *sequence list*, which contains a sequence of *stages*. Each stage specifies the buffer, its number of loops, and its *marker offset*.

Figure 2-4 illustrates the concepts of waveform samples, buffer, stage, staging list, and linking and looping. Waveform Sample A shows the concept of waveform samples used to create a waveform, shown in Waveform Buffer/Segment 1. In this example, Waveform Buffer/Segment 1 represents a single cycle of a sine wave, and the waveform samples in Sample A are 16-bit samples. Waveform Stage 1 shows a stage created from Buffer 1. Stage 1 is Buffer 1 with three cycle iterations.

Waveform Sample B shows samples for Waveform Buffer/Segment 2, which represents a triangular waveform. Waveform Stage 2 is created using two iterations of Buffer 2.

Stage 3 is created using a single iteration of Buffer 1. These waveforms are linked in a sequence, as shown in Figure 2-4. The concept of using a staging list to generate waveforms is referred to as *waveform linking and looping* or *waveform staging*.

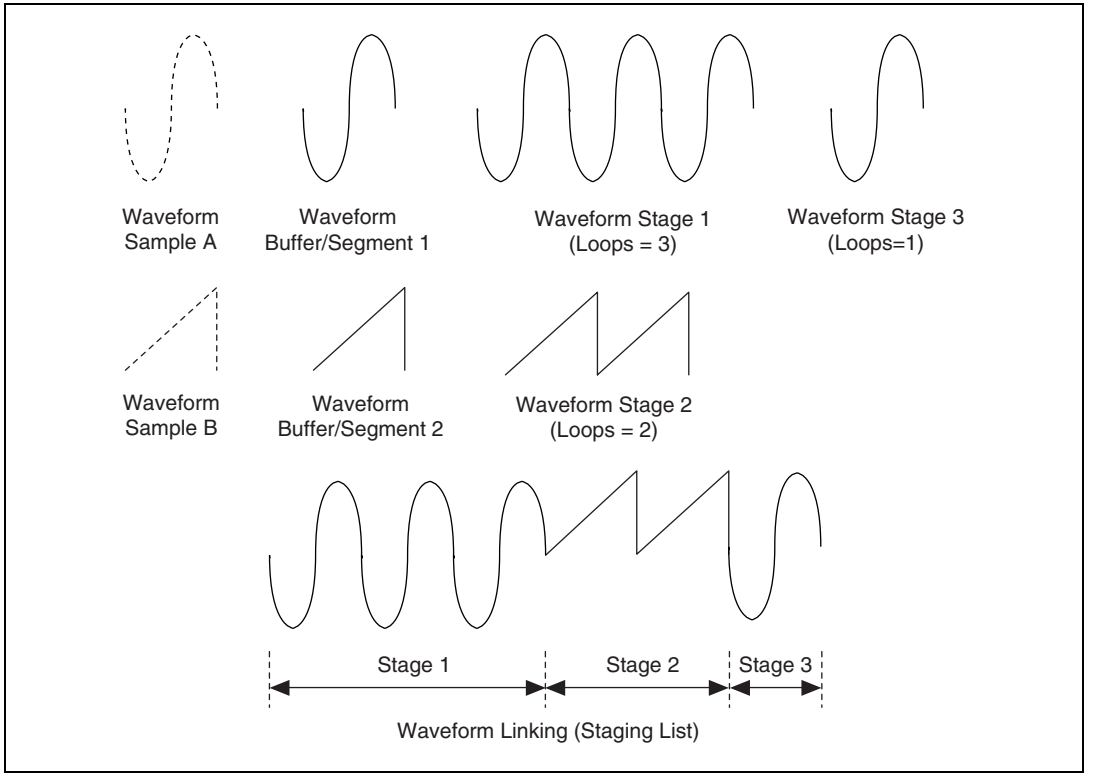

Figure 2-4. Waveform Linking and Looping

Waveform Staging

Figure 2-5 shows waveform staging in hardware. The instruction FIFO contains the staging list, which the NI 5411/5431 sequencer reads for waveform generation.

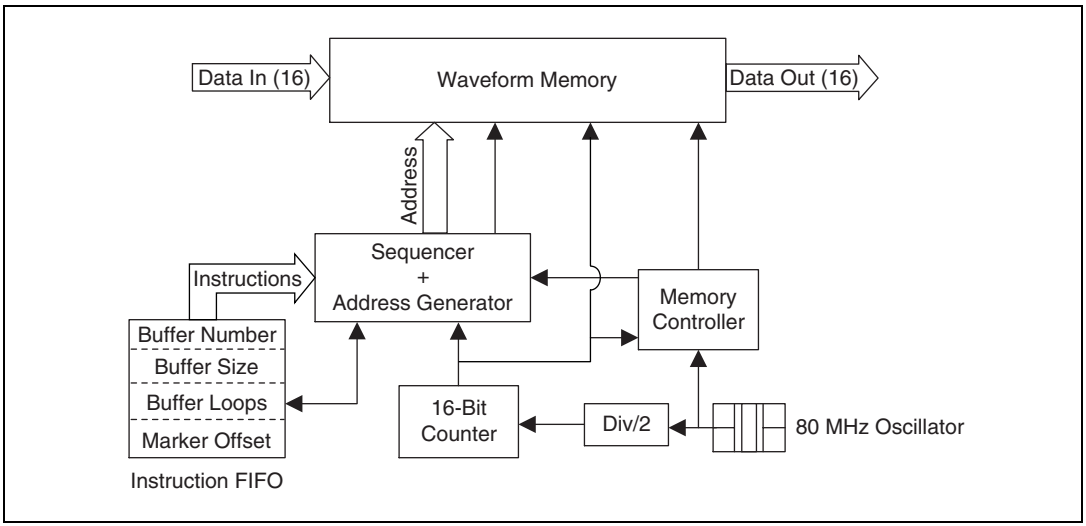

Figure 2-5. Waveform Staging Block Diagram

Each stage is made up of four instructions:

- *Buffer number*—Specifies the buffer number to be generated.
- *Buffer size*—Specifies the total count of the buffer to be generated. This count may not be the actual size of that buffer. If the count is less than the actual size of the buffer, only a part of that buffer is used for that stage. If the count is more than the actual size of that buffer, part of the next sequential buffer is also used. If the buffer size is set to zero, the software automatically uses the true size of that buffer.
- *Buffer loops*—Specifies the number of times that buffer has to be looped. The maximum number of loops possible is 65,535.
- *Marker offset*—Specifies where the marker must be generated within that buffer. For more information on markers, see the *Marker Output Signal* section later in this chapter.

Note The maximum number of waveform stages the instruction FIFO can store for Arb mode is 290.

Direct Digital Synthesis (DDS) Mode

Direct digital synthesis (DDS) is a technique for deriving, under digital control, an analog frequency source from a single reference clock frequency. This technique produces high-frequency accuracy and resolution, temperature stability, wideband tuning, and rapid and phase-continuous frequency switching. You should use DDS mode for standard function generation rather than for arbitrary waveform generation.

The NI 5411/5431 uses a 32-bit, high-speed accumulator with a lookup memory and a 12-bit DAC for DDS-based waveform generation. Figure 2-6 shows the building blocks for DDS-based waveform generation.

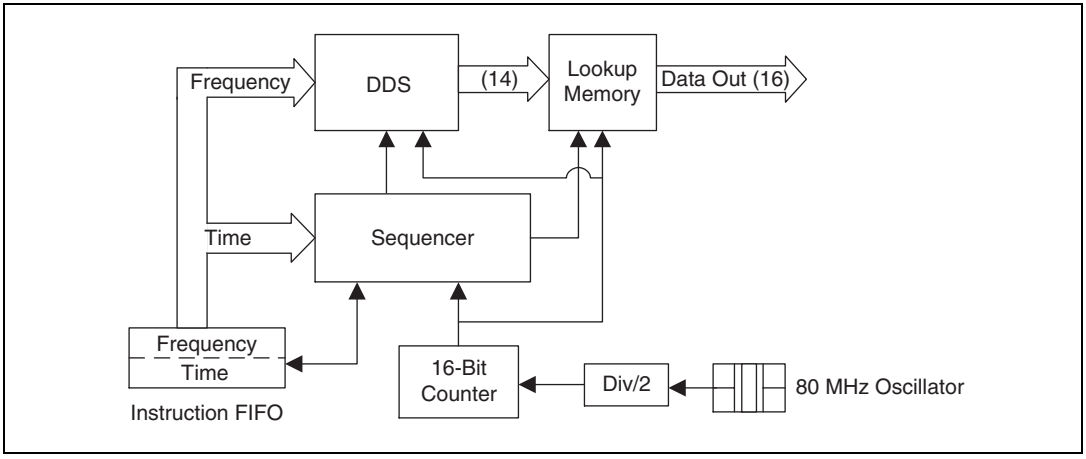

Figure 2-6. DDS Building Blocks

The lookup memory is dedicated to the DDS mode only and cannot be used in Arb mode. You can store one cycle of a repetitive waveform—a sine, triangular, square, or arbitrary wave—in the lookup memory. Then, you can change the frequency of that waveform by sending just one instruction. You can use DDS mode for very fine frequency resolution function generation. You can generate sine waves of up to 16 MHz for NI 5411 and 8 MHz for NI 5431 with a frequency resolution of 10.0 mHz. Because this mode uses an accumulator, waveform generation loops back to the beginning of the lookup memory after passing through the end of the lookup memory.

In this mode, each stage is made up of two instructions: the *frequency*, which specifies the frequency of the waveform to be generated, and the *time*, which specifies the time for which the frequency is to be generated.

Note You cannot specify the number of iterations for a waveform to be generated in DDS mode.

Frequency Hopping and Sweeping

You can define a staging list in DDS mode for performing *frequency hops and sweeps*. The entire staging list uses the same buffer loaded into the lookup memory. All stages differ in the frequency to be generated. As shown in Figure 2-6, a stage in DDS mode has a different instruction set than Arb mode.

Note The minimum time that a frequency should be generated is 2 µs. Therefore, the maximum hop rate from frequency to frequency is 500 kHz.

The maximum number of stages that can be stored in the instruction FIFO for DDS mode is 512. For more information on the waveform generation process, refer to your software documentation.

Triggering

You use triggering to start and step through a waveform generation. The trigger sources and modes of operation are explained in the following sections.

Trigger Sources

Trigger sources are software selectable. By default, the software produces the trigger sources. You can also use an external trigger from a pin on the digital I/O connector, the RTSI trigger lines on the RTSI bus, or the TTL trigger lines on the PXI trigger bus on the backplane. Figure 2-7 shows the trigger sources for the NI 5411/5431.

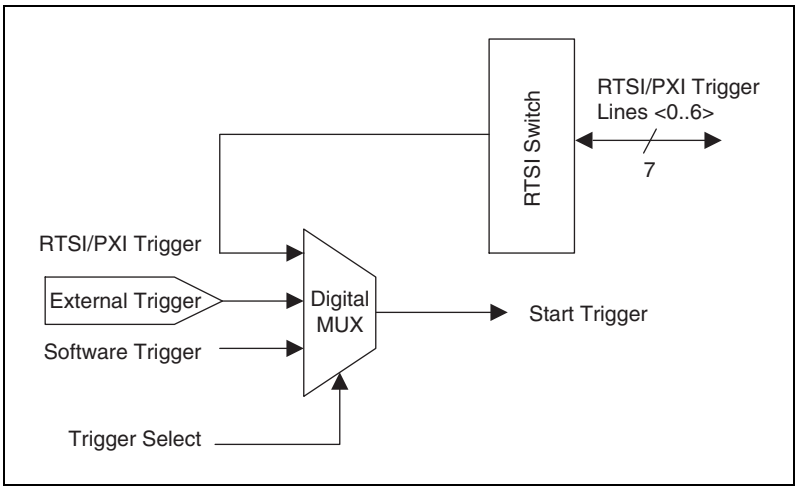

Figure 2-7. Waveform Generation Trigger Sources

If you need to automatically trigger the waveform generation, use software to generate the triggers. A rising TTL edge is required for external triggering.

For external triggering, apply a rising edge TTL signal to the EXT_TRIG input. This signal should remain deasserted (logic low) until after the waveform generation has been initiated in software.

For more information on triggering over RTSI lines, see the *RTSI/PXI Trigger Lines* section later in this chapter.

Modes of Operation

The NI 5411/5431 has four triggering modes—single, continuous, stepped, and burst. These trigger modes are available for both Arb and DDS modes.

Single Trigger Mode

The waveform you define in the staging list is generated only once by going through the entire staging list. Only one trigger is required to start the waveform generation.

You can use single trigger mode with both the Arb and DDS waveform generation modes as follows:

- Arb mode—Figure 2-8 uses the stages 1, 2, and 3 shown in Figure 2-4 to illustrate a single trigger mode of operation for Arb waveform generation mode. After the NI 5411/5431 receives a trigger, the

waveform generation starts at the first stage and continues through the last stage. The last stage is generated repeatedly until you stop the waveform generation.

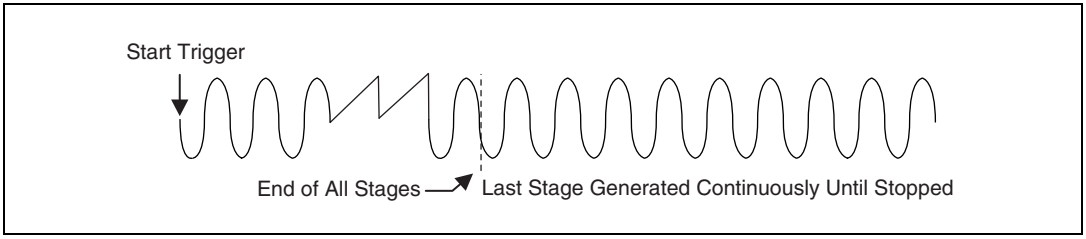

Figure 2-8. Single Trigger Mode for Arb Mode

Note You can settle to a predefined state by making the last stage emulate that state.

- DDS mode—After the NI 5411/5431 receives a trigger, the waveform generation starts at the first stage and continues through the last stage. The last stage is generated repeatedly until you stop the waveform generation. Figure 2-9 illustrates a single trigger mode of operation for DDS waveform generation mode.

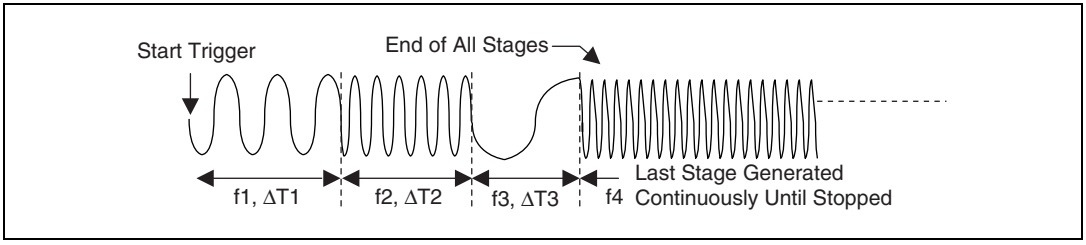

Figure 2-9. Single Trigger Mode for DDS Mode

For example, assume that one cycle of a sine wave is stored in the DDS lookup memory. For stage 1, f1 specifies the sine frequency to be generated for time ΔT1, f2 and ΔT2 for stage 2, and so on. If there are four stages in the staging list, f4 will be generated continuously until the waveform generation is stopped.

Continuous Trigger Mode

The waveform you define in the staging list is generated infinitely by continually cycling through the staging list. After a trigger is received, the waveform generation starts at the first stage, continues through the last stage, and loops back to the start of the first stage, continuing until you stop

the waveform generation. Only one trigger is required to start the waveform generation.

You can use continuous trigger mode with both the Arb and DDS waveform generation modes as follows:

- Arb mode—Figure 2-10 uses the stages shown in Figure 2-4 to illustrate a continuous trigger mode of operation for Arb waveform generation mode.

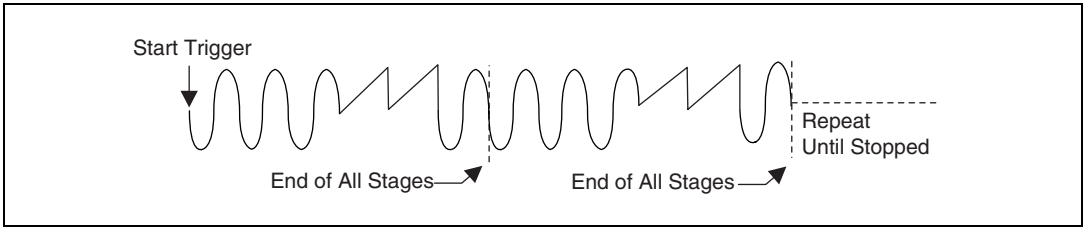

Figure 2-10. Continuous Trigger for Arb Mode

- DDS mode—Figure 2-11 illustrates a continuous trigger mode of operation for DDS waveform generation mode.

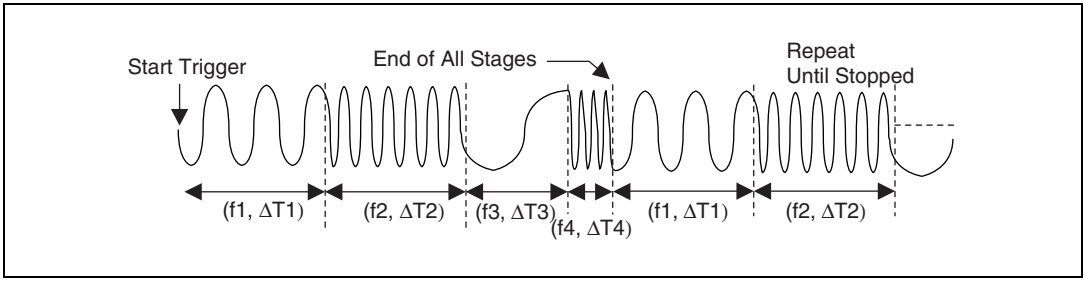

Figure 2-11. Continuous Trigger for DDS Mode

Stepped Trigger Mode

After a start trigger is received, the waveform defined by the first stage is generated. Then, the device waits for the next trigger signal. On the next trigger, the waveform described by the second stage is generated, and so on. Once the staging list is exhausted, the waveform generation returns to the first stage and continues in a cyclic fashion.

You can use the stepped trigger mode with both the Arb and DDS waveform generation modes as follows:

- Arb mode—Figure 2-12 uses the stages shown in Figure 2-4 to illustrate a stepped trigger mode of operation for the Arb mode. If a trigger is received while a stage is being generated, the trigger is ignored. A trigger is recognized only after the stage has been completely generated.

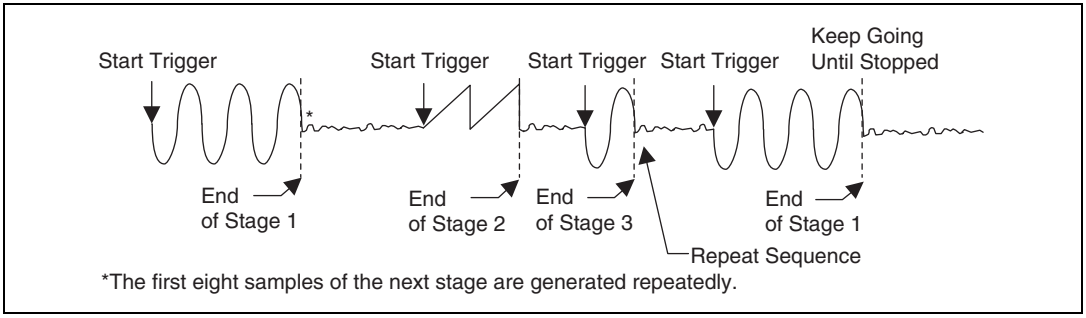

Figure 2-12. Stepped Trigger Mode for Arb Mode

After any stage has been generated completely, the first eight samples of the next stage are repeated continuously until the next trigger is received.

Note For stepped trigger mode, you can predefine the state in which a stage ends by making the first eight samples of the next stage represent the state you want to settle.

- DDS mode—When using the DDS mode of waveform generation, stepped trigger mode operates the same as burst trigger mode, which is described in the following section.

Burst Trigger Mode

After a start trigger is received, the waveform defined by the first stage buffer is generated until another trigger is received. At the next trigger, the buffer of the previous stage is completed before the waveform defined by the second stage buffer is generated. Once the staging list is exhausted, the waveform generation returns to the first stage and continues in a cyclic fashion.

You can use burst trigger mode with both the Arb and DDS waveform generation modes as follows:

- Arb mode—Figure 2-13 uses the stages shown in Figure 2-4 to illustrate a burst trigger mode of operation for Arb mode. In this mode, the loop information associated with each stage is not used. The trigger causes the generation to proceed to the next stage once the previous buffer is completed.

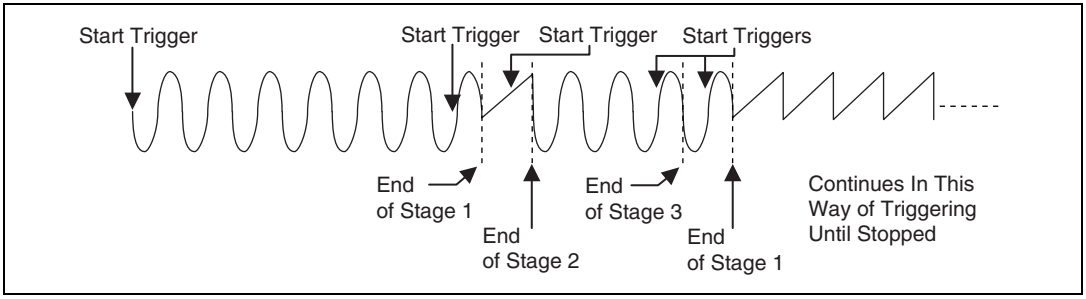

Figure 2-13. Burst Trigger Mode for Arb Mode

- DDS mode—Figure 2-14 illustrates a burst trigger mode of operation for DDS mode. Switching from stage to stage is phase continuous. In this mode, the time instruction is not used. The trigger paces the waveform generation from one frequency to the other.

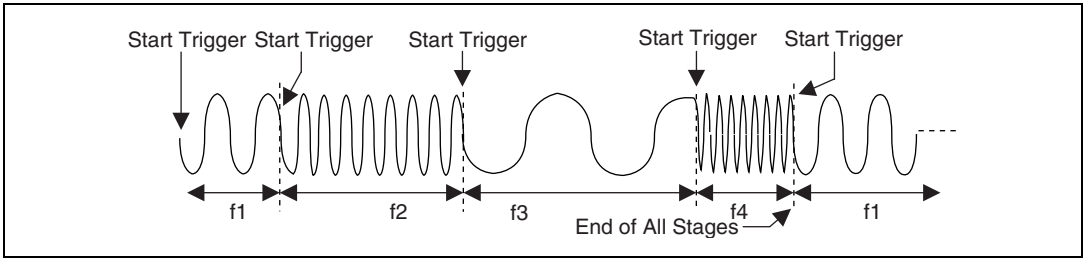

Figure 2-14. Burst Trigger Mode for DDS Mode

Marker Output Signal

A marker, which is equivalent to a trigger output signal, is available on a separate pin in the digital I/O connector. You can define this TTL-level trigger output signal at any position in the waveform buffer. You can place a marker in every stage; however, only one marker per stage is allowed.

You can specify a marker by giving an offset count (in number of samples) from the start of the waveform buffer specified by the stage. If the offset is out of range of the number of samples in that stage, the marker does not appear at the output. If the buffer is looped multiple times in a stage, the marker is generated that many times.

Note The marker begins generating on the last sample preceding the specified placement that is evenly divisible by eight and is generated for eight update clocks. Therefore, the beginning of the marker is always within eight samples of the specified placement.

If you want a marker at an offset of zero from the start of the waveform buffer, the marker is eight samples long beginning with the first sample. A marker at an offset of seven from the start of the waveform buffer is also eight samples long beginning with the first sample, as shown in Table 2-1. A marker at an offset of eight is generated at positions 8–15.

Table 2-1. Generated Marker Positions

Marker Requested	Marker Generated
At sample 0 from the beginning of the buffer	Sample position 0–7
At sample 1 from the beginning of the buffer	Sample position 0–7
At sample 7 from the beginning of the buffer	Sample position 0–7
At sample 8 from the beginning of the buffer	Sample position 8–15
At sample 27 from the beginning of the buffer	Sample position 24–31
At sample 255 from the beginning of the buffer	Sample position 248–255

Figure 2-15 shows an analog waveform being generated at one connector and a marker being generated at another I/O connector. Point A shows a marker generated for requested positions 0–7, and point B shows a marker generated for requested positions of 8–15.

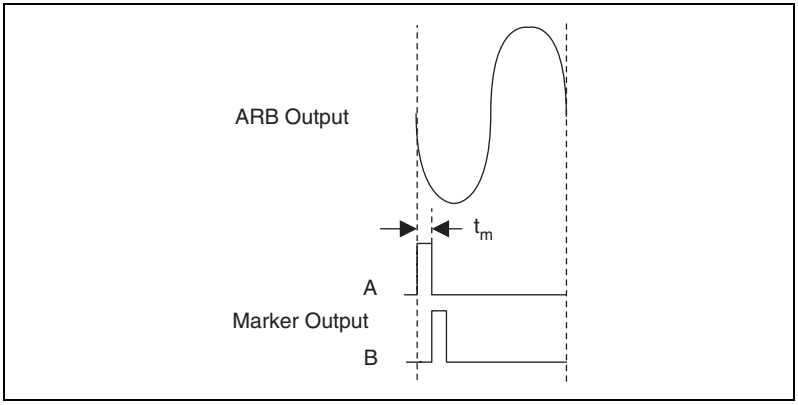

Figure 2-15. Markers as Trigger Outputs

Note Marker output signals are an important feature to trigger other instruments or devices at a specified time while a waveform generation is in progress.

Application of Markers

There is a delay of more than 76 sample clocks from the external trigger (EXT_TRIG) edge to the analog waveform generation on the output connector. Therefore, synchronizing the NI 5411 output signal to other devices with faster and predictable trigger response times is difficult. For such applications, use the marker from the NI 5411 as the trigger source for the other device. You may do this over the RTSI bus, PXI trigger lines, or externally on the connector.

Analog Output

Analog waveforms are generated as follows:

1. The 12-bit digital waveform data is fed to a high-speed DAC.
2. A *lowpass filter* filters the DAC output.
3. This filtered signal is amplified before it goes to a 10 dB attenuator.

Note The DAC output can be fine-tuned for gain and offset. Since the offset is adjusted before the main attenuators and amplifier, it is referred to as *pre-attenuation offset*. This fine-tuning of gain and offset is performed by separate DACs.

4. The output from the 10 dB attenuator then goes to the main amplifier, which can provide up to ±5 V levels into 50 Ω. An output relay can switch between ground level and the main amplifier. Refer to the

Output Enable section of this document for additional information about this relay.

5. The output of this relay goes to a series of passive attenuators.
6. The output of the attenuators goes through a selectable output impedance of 50 or 75 Ω to the I/O connector.

Figure 2-16 shows the essential block diagram of analog waveform generation.

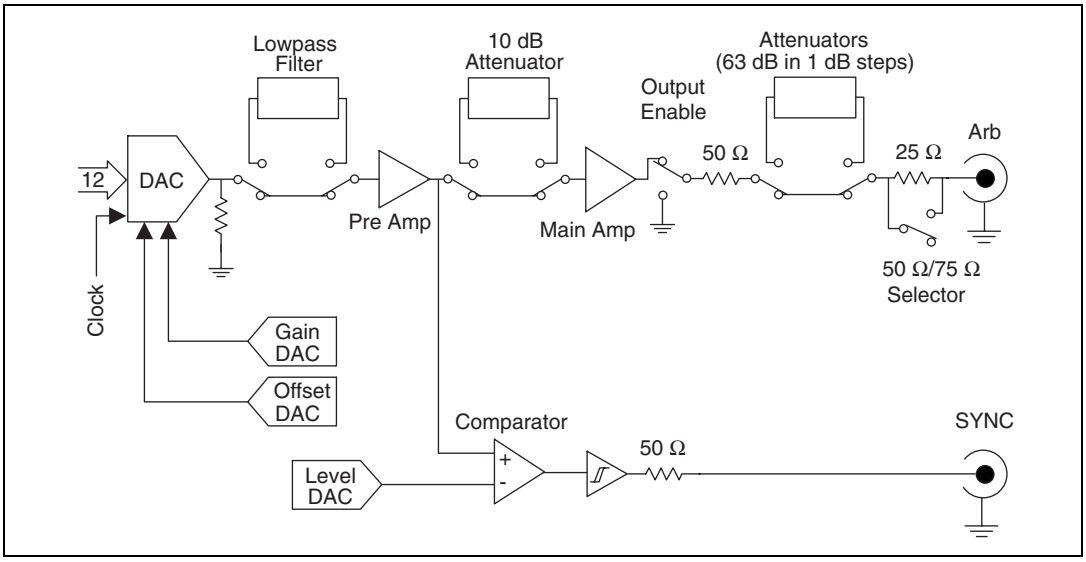

Figure 2-16. Analog Output and SYNC Out Block Diagram

Figure 2-17 shows the timing relationships of the trigger input, waveform output, and marker output. T_{d1} is the pulse width on the trigger signal. T_{d2} is the time delay from trigger to output on Arb output. T_{d3} is the time between the marker output and Arb output. T_{d4} is the pulse width on marker output. Refer to Appendix A, *Specifications*, for more information on these timing parameters.

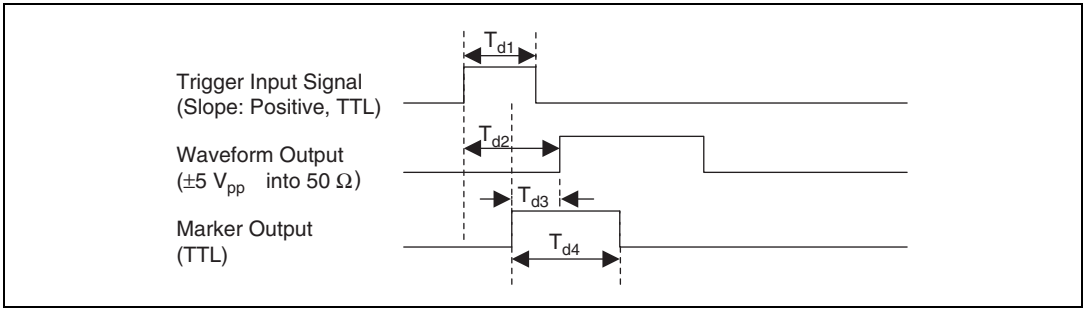

Figure 2-17. Waveform, Trigger, and Marker Timings

Note You can switch off the analog lowpass filter at any time during waveform generation. When you change this setting, the bouncing of electromechanical relays on the NI 5411/5431 distorts the output signal for about 10 ms.

SYNC Output and Duty Cycle

The SYNC output is a TTL version of the sine waveform generated at the output. The signal from the pre-amplifier is sent to a comparator, where it is compared against a level set by the *level DAC*. The output of this comparator is sent to the SYNC connector through a hysteresis buffer and a 50 Ω series resistor to reverse terminate reflected pulses.

You can use the SYNC output as a very high-frequency resolution, software-programmable clock source for many applications. You also can vary the duty cycle of SYNC output, on the fly, by changing the output of the level DAC. The SYNC output might not carry meaning for other types of generated waveforms.

Note You can change the duty cycle of the SYNC output at any time during waveform generation.

Output Attenuation

Figure 2-18 shows the NI 5411/5431 output attenuator chain. The output attenuators are made of resistor networks and may be switched in any combination. The maximum attenuation possible on the NI 5411/5431 is 73 dB.

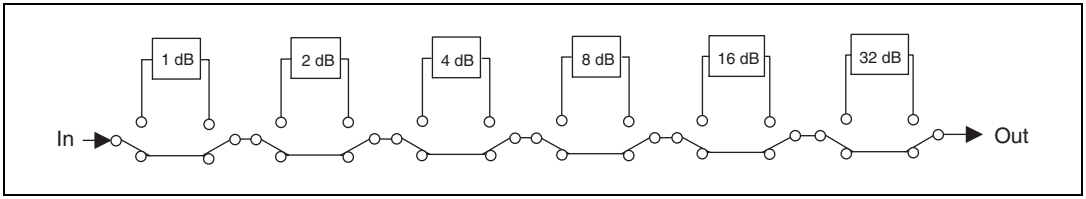

Figure 2-18. Output Attenuation Chain

By attenuating the output signal, you keep the *dynamic range* of the DAC; that is, you do not lose any bits from the digital representation of the signal because the attenuation is done after the DAC and not before it.

$$\text{attenuation (in decibels)} = -20 \log_{10} (V_o / V_i)$$

where V_o = desired voltage level for the output signal
V_i = input voltage level.

Note For the NI 5411/5431, $V_i = \pm 5$ V for a terminated load and ±10 V for an unterminated load.

NI-FGEN calculates the value of the output attenuation chain, which you can control by changing the gain or peak-to-peak amplitude parameters. 0 dB attenuation corresponds to a gain of 5 V or an amplitude of 10 $V_{pk\text{-}pk}$. The maximum attenuation of 73 dB corresponds to a gain of 1.12 mV or an amplitude of 2.24 $mV_{pk\text{-}pk}$. Any gain or amplitude less then this is coerced to this value.

Note You can change the output attenuation at any time during waveform generation. When you change this setting, the bouncing of electromechanical relays on the NI 5411/5431 distorts the output signal for about 10 ms.

Output Impedance

As shown in Figure 2-18, before the signal reaches the output connector, you can select an output impedance of 50 Ω or 75 Ω. If the load impedance is 50 Ω and all the attenuators are off (an output attenuation of 0 dB), the output levels are ±5 V.

Most applications use a load impedance of 50 Ω, but applications such as video device testers require 75 Ω. If the load is a very high-input impedance load (~1 MΩ), you will see output levels up to ±10 V.

Note You can change the output impedance at any time during waveform generation. When you change this setting, the bouncing of electromechanical relays on the NI 5411/5431 distorts the output signal for about 10 ms.

Output Enable

You can switch off the waveform generation at the output connector by controlling the *output enable relay*, as shown in Figure 2-16. When the output enable relay is off, the output signal level goes to ground level.

Note Even though the output enable relay is in the off position, the waveform generation process continues internally on the NI 5411/5431.

You can use this feature to disconnect and connect different devices to the NI 5411/5431 on the fly.

Note You can change the output enable state at any time during waveform generation. When you change this setting, the bouncing of electromechanical relays on the NI 5411/5431 distorts the output signal for about 10 ms.

Pre-Attenuation Offset

The NI 5411/5431 hardware supports a DC offset of up to ±2.5 V before the attenuation chain. Unless the 10 dB attenuator is switched in, which occurs when the gain is less than 1.58 V or the amplitude is less then 3.16 $V_{pk\text{-}pk}$, the waveform maximum plus the offset must not exceed ±5 V into 50 Ω. If it does, the waveform is clipped. Refer to Figure 2-16 for a diagram showing the location of the 10 dB attenuator.

NI-FGEN automatically calculates the pre-attenuation offset value based on the DC offset and gain or amplitude values, so the allowable DC offset range is dependent on the amplitude. For example, if you have a gain of 0.5 V or an amplitude of 1 $V_{pk\text{-}pk}$, the maximum DC offset you can apply is 0.25 V, which corresponds to a pre-attenuation offset of 2.5 V.

Note You can change the DC Offset at any time during waveform generation. Refer to your software documentation for additional information.

External and High-Resolution Clocking (NI 5411/5431 for PXI Only)

You can connect an external clock to the PLL Ref input connector of your NI 5411/5431 for PXI. To do this, however, you have to set up your clock source in the software. Refer to the software documentation for information on setting up your clock. This external clock can be used as the update clock. The maximum frequency of the external clock is 40 MHz.

You must not change the frequency of this clock during waveform generation (sweeping of external clock is not allowed). This may result in malfunctioning of the board. Change the clock's frequency only before initiating the waveform generation. If any malfunction occurs, stop the waveform generation and reset the board to a known state before restarting.

These boards also support an internal high-resolution clocking mode. When you use this type of clock, you can set the update clock frequency to any value from 0 to 40 MHz with a resolution of approximately 40 mHz. This mode is useful for applications that require a precise clock source, which is not possible using the default counter-based clocking scheme. Use this feature for applications such as CDMA, GSM, and ADSL waveform generation.

Digital Filter Considerations

When you use external or high-resolution clocking, the actual update rate depends on the state of the digital filter.

For external clocking, if the digital filter is enabled, the actual update rate equals half the frequency of the external clock. In this case, the maximum frequency of the external clock is 40 MHz and the corresponding update rate achieved is 20 MHz. If the digital filter is disabled, the actual update rate equals the frequency of the external clock. In this case, the maximum frequency of the external clock is 40 MHz and the corresponding update rate achieved is also 40 MHz.

For high-resolution clocking, when the digital filter is enabled, the update rate is limited to 20 MHz. NI-FGEN reports an error if the digital filter is enabled and the user specifies an update rate greater than 20 MHz while high-resolution clocking is in use. If the digital filter is disabled and high-resolution clocking is in use, the maximum update rate allowed is 40 MHz.

Phase-Locked Loops and Board Synchronization (NI 5411 Only)

Figure 2-19 illustrates the block diagram for the NI 5411 for PCI/ISA PLL circuit. Figure 2-20 illustrates the block diagram for the NI 5411 for PXI PLL circuit. The PLL consists of a voltage-controlled crystal oscillator (VCXO) with a tuning range of ±100 ppm. This VCXO generates the main clock of 80 MHz.

The PLL can lock to a reference clock source from the external connector, from a RTSI Osc line on the RTSI bus (NI 5411 for PCI/ISA), or from a 10 MHz Osc line on the PXI backplane bus (for NI 5411 for PXI). The PLL can also be tuned internally using a calibration DAC (CalDAC). National Instruments accurately performs this tuning during manufacturing. Refer to the *RTSI/PXI Trigger Lines* section later in this manual for additional information on using the RTSI and 10 MHz Osc lines.

The reference and VCXO clock are compared by a phase comparator running at 1 MHz. The loop filters the error signal and sends it to the control pin of the VCXO to complete the loop.

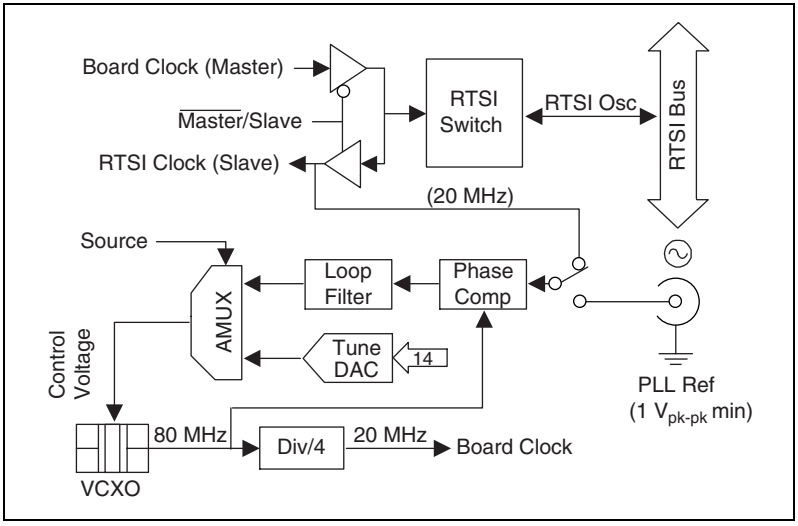

Figure 2-19. PLL Architecture for the NI 5411 for PCI/ISA

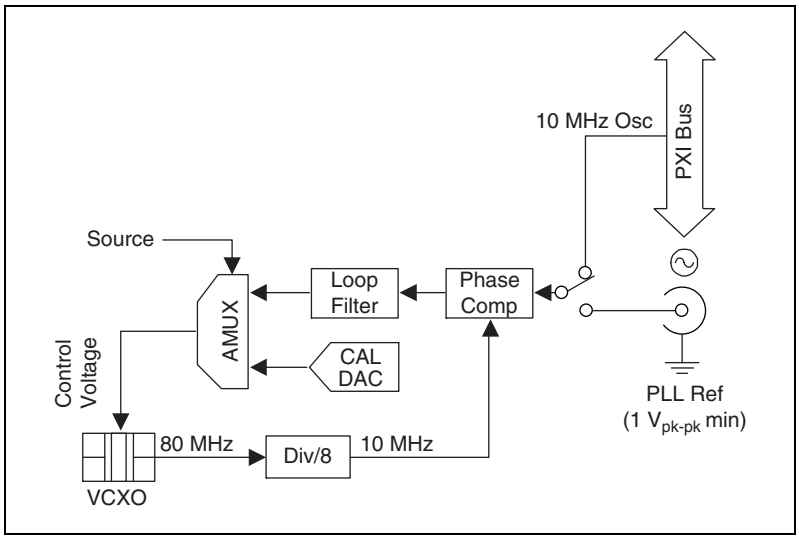

Figure 2-20. PLL Architecture for the NI 5411 for PXI

You can phase lock to an external reference clock source of 1 MHz and from 5–20 MHz in 1 MHz increments. The PLL can lock to a signal level of at least 1 V_{pk-pk}.

Caution Do not increase the voltage level of the clock signal at the PLL reference input connector by more than the specified limit, 5 V_{pk-pk}.

- NI 5411 for PCI/ISA

  The VCXO output of 80 MHz is further divided by four to send a 20 MHz board clock signal to the RTSI bus.

Master/Slave Operation

You can phase lock the NI 5411 to other devices or other NI 5411 devices in two different ways—as shown in Figure 2-21—to synchronize multiple devices in a test system.

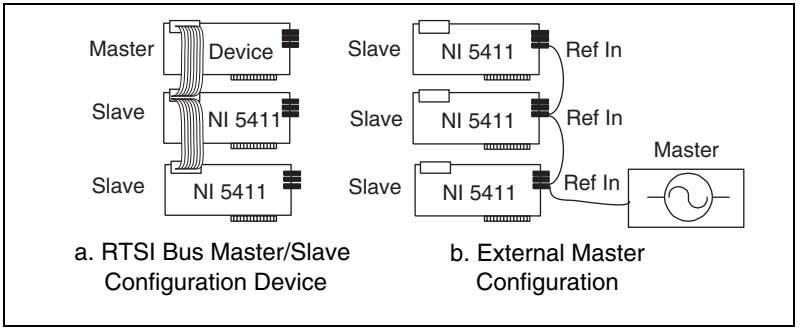

Figure 2-21. Master/Slave Configurations for Phase Locking

- NI 5411 for PCI/ISA

Example 1, in Figure 2-21a, shows any National Instruments device with RTSI bus capability as the master. To phase lock NI 5411s for PCI/ISA to this master, perform the following steps in software:

1. Set the National Instruments device (master) to send a 20 MHz signal over the RTSI bus on the RTSI Osc line. If this device is a NI 5411, set the source for the RTSI clock line to `Board_clock` for NI-FGEN software and `internal` for LabVIEW.
2. Set up the slave devices so that the PLL reference source is set to the RTSI clock line.
3. Set the PLL reference frequency parameter to 20 MHz. The boards are now frequency locked to the master.
4. To further phase lock the boards, set up the master to send the trigger signal on one of the RTSI trigger lines.
5. Set up the slave devices to receive their trigger signal on the RTSI bus.
6. Start the waveform generation on all the slaves.
7. Start the waveform generation on the master.

The master triggers all the slaves that are phase and frequency locked to each other and the master.

Example 2, in Figure 2-21b, shows an external device as the master. To phase lock the NI 5411 devices to this master, perform the following steps:

1. Set the master device to send any valid reference clock to the PLL reference input connector.
2. Set up the slave devices with the PLL reference source set to the I/O connector.
3. Set the PLL reference frequency parameter to the clock frequency sent by the master. The boards are now frequency locked to the master.
4. To further phase lock the boards, connect the trigger source to the trigger input of the 50-pin digital connectors of all the boards, and set up the slaves to receive the triggers on trigger input connector.
5. Start the waveform generation on all the slaves.
6. Activate the external trigger signal. All the slaves are triggered at the same time and are phase and frequency locked.

- NI 5411 for PXI

To phase lock NI 5411s for PXI, perform the following steps:

1. Set all the NI 5411s to accept the 10 MHz Osc line on the PXI backplane as the PLL reference clock signal.
2. Set the PLL reference frequency to 10 MHz. The boards are now frequency locked to the backplane 10 MHz Osc line.
3. Choose the sample update clock source to be internal divide-down mode, high-resolution mode, or external. External clocking mode results in the best synchronization.
4. To further phase lock the boards, set up the master to send the trigger signal on one of the PXI trigger lines.
5. Set up the slaves to receive their trigger signal on the PXI trigger bus.
6. Set up the master to send the `Board_SYNC` signal on the PXI trigger line and the slaves to receive the `Board_SYNC` signal on the same PXI trigger line.
7. Start the waveform generation on all the slaves.
8. Start the waveform generation on the master.

The master triggers all the slaves, which are phase and frequency locked to each other and the master.

Note If two or more NI 5411 devices are running in Arb mode and are locked to each other using the same reference clock, you see a maximum phase difference of one sample clock on the locked boards when they are triggered at the same time.

Note If two or more NI 5411 devices are running in DDS mode and are locked to each other using the same reference clock, they are frequency locked, but the phase relationship is indeterminate.

Analog Filter Correction

The NI 5411/5431 can correct for slight deviations in the flatness of the frequency characteristic of the analog lowpass filter in its *passband*, as shown in Figure 2-22. Curve A shows a typical lowpass filter curve. The response of the filter is stored in an onboard *EEPROM* in 1 MHz increments up to 16 MHz for NI 5411 and up to 8 MHz for NI 5431. Curve C is the correction applied to the frequency response. The resulting Curve B is a flat response over the entire passband. If you want to generate a sine wave at a particular frequency with filter correction applied, you have to specify that frequency through your software.

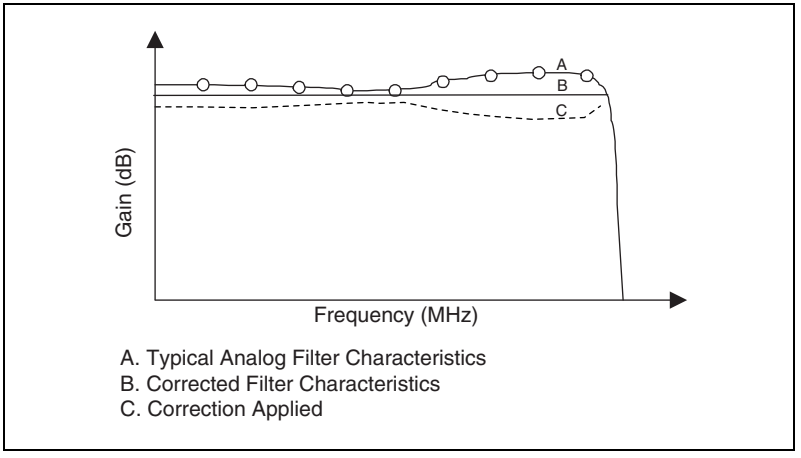

Figure 2-22. Analog Filter Correction

Note You can change the filter frequency correction at any time during waveform generation.

Digital Pattern Generation

The NI 5411/5431 has 16-bit digital pattern generation outputs at the digital connector. This digital data is first synchronized to the sample clock and then buffered and sent to the connector through a 68 Ω series resistor. The sample clock is also buffered and sent to the digital connector to *latch* the data externally. Figure 2-23 shows the data path for digital pattern generation. Since the digital pattern data does not go through the digital filter, it is available directly from the memory. This means that there is a fixed delay of 26 sample clocks between the analog waveform (which lags behind the digital waveform) and the digital patterns. Although the digital filter can be disabled in software, there will still be a 26 sample clock delay.

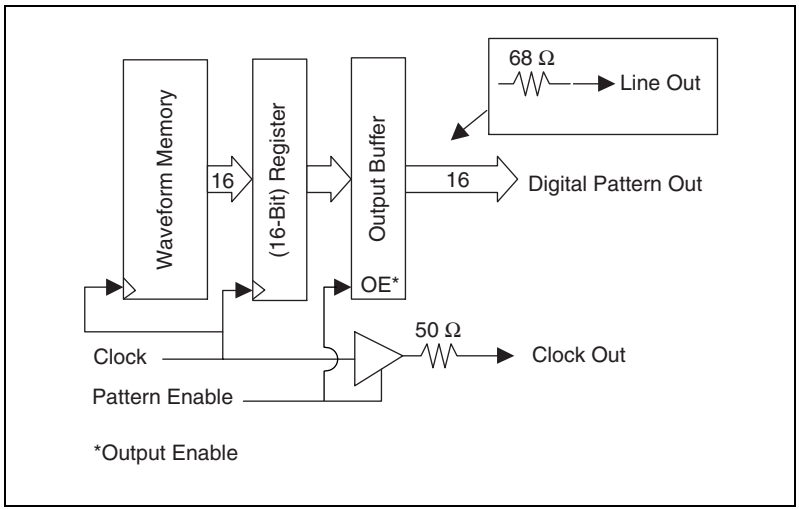

Figure 2-23. Digital Pattern Generator Data Path

You can enable or disable digital pattern generation through software. All linking and looping capabilities are available for digital pattern generation as well. If you select DDS mode, the DDS data appears at the digital I/O connector.

You can use digital pattern generation to test digital devices such as serial and parallel DACs and to emulate protocols.

Note At computer power-up and reset, digital pattern generation is disabled.

Figure 2-24 shows the timing waveforms for digital pattern generation; t_{clk} is the clock time period and t_{co} is the time delay from clock to output on

pattern lines, such as PA<0..15>. Refer to Appendix A, *Specifications*, for these timing parameters.

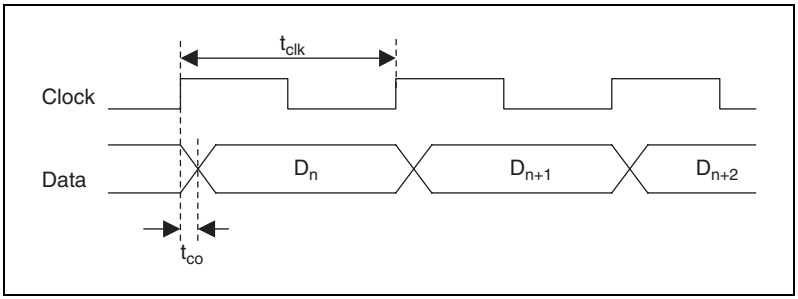

Figure 2-24. Digital Pattern Generation Timing

The sample clock for integral subdivisions of 40 MHz always has a high pulse width of 25 ns. If the t_{co} time is insufficient for the hold time of your device, you can use the falling edge of the sample clock output (PCLK) to register the digital pattern data.

RTSI/PXI Trigger Lines

The NI 5411/5431 for PCI/ISA contains seven trigger lines and one RTSI clock line available over the RTSI bus to send and receive NI 5411/5431-specific information to other boards that have RTSI connectors. Figure 2-25 shows the RTSI trigger lines and routing of NI 5411/5431 for PCI/ISA signals to the RTSI switch.

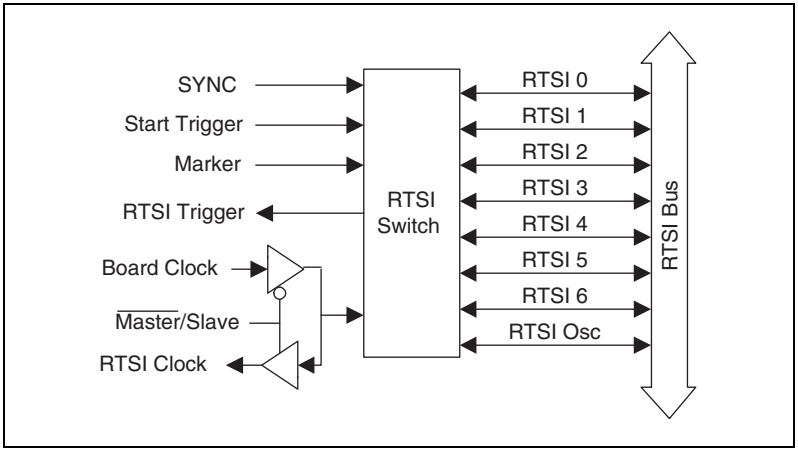

Figure 2-25. RTSI Trigger Lines and Routing for the NI 5411/5431 for PCI/ISA

Figure 2-26 shows the PXI trigger lines and routing of NI 5411/5431 for PXI signals to the RTSI switch.

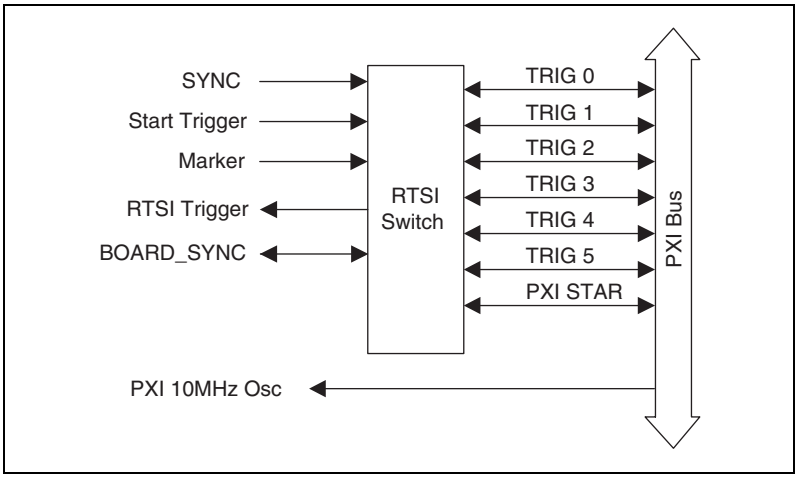

Figure 2-26. PXI Trigger Lines, 10 MHz Backplane Oscillator, and Routing for the NI 5411/5431 for PXI

The NI 5411/5431 can receive a hardware trigger from another board as a RTSI trigger signal on any of the RTSI/PXI trigger lines.

You can also route signals as follows:

- Route the marker generated during waveform generation in Arb mode to any of the RTSI/PXI bus trigger lines.
- Route the Start Trigger signal generated on the NI 5411/5431 to other boards through any of the RTSI/PXI bus trigger lines.
- Route the SYNC output generated on the NI 5411/5431 to other boards through any of the RTSI/PXI bus trigger lines.You can use this signal to give other boards an accurate and fine frequency resolution clock.

♦ NI 5411 for PCI/ISA

For phase locking to other boards as a master, the NI 5411 sends an onboard 20 MHz signal to the RTSI Osc line as a board clock signal. For locking to other devices as a slave, the NI 5411 receives the RTSI Osc line as a RTSI clock signal.

- NI 5411 for PXI

  For phase locking to other boards, the NI 5411 for PXI receives the PXI backplane 10 MHz Osc as a reference clock signal. All the NI 5411s for PXI use this common signal as the reference clock for phase locking.

  The bidirectional `Board_SYNC` signal is used as a trigger signal to synchronize multiple boards only during a master/slave operation (see the *Master/Slave Operation* section earlier in this chapter). For general-purpose triggering, you must use either Start Trigger for the outgoing trigger or RTSI Trigger for the incoming trigger.

- NI 5431 for PCI/PXI

  Phase locking multiple NI 5431s is not supported.

Note Refer to your software documentation for selecting and routing signals to the RTSI/PXI trigger bus.

Calibration

Calibration is the process of minimizing measurement errors by making small circuit adjustments. On the NI 5411/5431, NI-FGEN automatically makes these adjustments by retrieving predetermined constants from the onboard EEPROM, calculating correction values, and writing those values to the CalDACs.

National Instruments calibrates all NI 5411/5431 devices to the levels indicated in Appendix A, *Specifications*. Factory calibration involves procedures such as nulling the offset and gain errors. However, since offset and gain errors may drift with time and temperature, you may need to recalibrate your device. Contact National Instruments to recalibrate your NI 5411/5431.

A

Specifications

This appendix lists the specifications for the NI 5411 and the NI 5431. These specifications are typical at 25 °C unless otherwise stated. The operating temperature range is 0 to 50 °C.

Analog Output

Number of channels 1

Resolution ..... 12 bits

Maximum update rate ..... 40 MHz

DDS accumulator ..... 32 bits

Frequency range

Waveform Type	NI 5411	NI 5431
Arb	40 MS/s	40 MS/s
PAL-B	—	40 MS/s
NTSC	—	40.02797 MS/s
PAL-M	—	40.009739 MS/s
Sine	16 MHz, max	8 MHz, max
SYNC (TTL)	16 MHz, max	8 MHz, max
Square	1 MHz, max	1 MHz, max
Ramp	1 MHz, max	1 MHz, max
Triangle	1 MHz, max	1 MHz, max

Frequency resolution (DDS mode) ..... 9.31 mHz

Voltage Output

Ranges.....±5 V into a 50 Ω load
±10 V into a high-impedance load

Accuracy.....±0.1 dB

Output attenuation.....0 to 73 dB
Resolution.....0.001 dB steps

Pre-attenuation offset
Range.....±2.5 V into 50 Ω[1]
Accuracy.....±5 mV

Output coupling.....DC

Output impedance.....50 Ω or 75 Ω software selectable

Load impedance.....50 Ω or greater

Output enable.....Software switchable

Protection.....Short-circuit protected

Sine Spectral Purity

Harmonic products and spurs
Up to 1 MHz.....–60 dBc
Up to 16 MHz.....–35 dBc

Phase noise.....–105 dBc/Hz at 10 kHz from carrier

[1] With less than 10 dB of attenuation, signal maximum plus offset (before attenuation) must not exceed ±5 V (into 50 Ω)

Filter Characteristics

Digital

- Type ..... Half-band interpolating
- Selection..... Software switchable (enable or disable)
- Taps 67
- Filter coefficients ..... Fixed 20-bit
- Data interpolating frequency ..... 80 MS/s
- Pipeline signal delay ..... 26 sampling periods

Analog

- Type ..... 7th-order L-C lowpass filter
- Passband ripple ..... ±2 dB

Waveform Specifications

Memory

- Arb mode
  - NI 5411 ..... 2,000,000 16-bit samples
  - NI 5431 ..... 8,000,000 16-bit samples
- DDS mode..... 16,384 16-bit samples

Segment length

- Arb mode ..... 256 samples minimum, multiples of eight samples
- DDS mode..... 16,384 samples, exact

Max segments in waveform memory..... 5,000 (Arb mode only)

Segment linking (instruction FIFO)

- Arb mode ..... 292 links
- DDS mode..... 512 links

Segment looping (Arb mode only)

- Count ..... 65,536 loops

Timing I/O

Update clock .....Internal, 40 MHz max
Interval count.....2 to 65,535

Phase locking
External reference sources.....Input connector, RTSI clock line, or internal
Reference clock frequencies.....1 MHz, 5–20 MHz in 1 MHz steps
Frequency locking range
NI 5411.....±100 ppm
NI 5431.....±500 ppm

Triggers

Digital Trigger

Compatibility .....TTL

Response .....Rising edge

Pulse width (T_{d1}).....20 ns min

Trigger to waveform output
(Arb mode) delay (T_{d2}).....76 sample clocks + 38 ns max

Trigger to waveform output
(DDS mode) delay (T_{d2}) .....28 sample clocks + 150 ns max

RTSI

Trigger lines 7

Clock lines 1

Bus Interface

Type .....Slave

Operational Modes

Type .....Single, continuous, burst, stepped

Other Outputs

SYNC Out

Level ..... TTL

Duty cycle ..... 20% to 80%, software controllable

Marker Output

Types ..... TTL

Location ..... User defined, one per stage

Pulse width (T_{d4}) ..... 8 sample clock periods

Arb output delay from marker (T_{d3})..... 50 ns max

Digital Pattern Output

Sample rate..... 40 MHz max

Resolution ..... 16 bits

Sample clock logic ..... TTL

Clock pulse HIGH time..... 25 ns fixed (for clock interval counts > 1)

PCLK to pattern data output time (T_{co})..... 1 ns max

Digital pattern logic ..... TTL

Logic level output ratings for SYNC, marker, digital pattern, and sample clock outputs

Type	Min	Max
V_{OH}	3.0 V	—
V_{OL}	—	0.7 V
I_{OH}	—	1.0 mA
I_{OL}	—	1.0 mA

V_{OH} = voltage output for logic level 1
V_{OL} = voltage output for logic level 0
I_{OH} = current output for logic level 1
I_{OL} = current output for logic level 0

External PLL Reference Input

Frequency .....1 MHz or 5–20 MHz in 1 MHz steps

Amplitude .....1 V_{pk-pk} ≤ level ≤ 5 V_{pk-pk}

Internal Clock

Frequency .....40 MHz

Initial accuracy .....±5 ppm

Temperature stability (0 to 5 °C).....±25 ppm

Aging (1 year).....±5 ppm

External Clock Reference Input

Frequency .....40 MHz, max

Amplitude .....TTL

Mechanical

Connectors

- ARB/Video (output) .....SMB/BNC
- SYNC (output).....SMB/BNC
- PLL reference (input) .....SMB
- Digital I/O (digital pattern out, marker out, external trigger in).....50-pin digital, SMB (for PXI)

Size .....1 slot

Power requirements .....5 V, 3.5 A max
12 V, 125 mA

B

Optional Accessories

National Instruments offers a variety of products to use with your NI 5411/5431, including probes, cables, and other accessories:

- Shielded and unshielded I/O connector blocks (SCB-68, TBX-68, CB-68)
- 16 MB memory module (optional)
- RTSI bus cables

For more specific information about these products, refer to your National Instruments catalogue or web site, or call the office nearest you.

Installing the Optional Memory Module (NI 5411 Only)

The standard onboard memory for the NI 5411 is 4 MB. You can upgrade to a 16 MB memory module to store large waveform buffers directly on the card. Perform the following steps to install the new memory module:

1. Turn off the computer and remove the top cover or access port to the I/O channel.
2. Unscrew the bracket and remove the NI 5411 from the slot it has been plugged into.
3. Gently place your NI 5411 on a flat surface with the component and memory module side facing up.
4. Unfasten the two screws on the side of the memory module.
5. Gently unplug the memory module from the main board and store the old memory module in an antistatic bag to avoid damage to the components.
6. Properly align the new 16 MB memory module over the connectors and plug it into the connectors.
7. Fasten the two screws you removed in step 4.
8. Follow the regular installation steps described in the *Where to Start with Your NI 5411* document.

Cabling

The following list gives recommended part numbers for cables that you can use with your NI 5411/5431 device:

- BNC male to BNC male, 50 Ω cable from ITT Pomona Electronics (part number BNC-C-xx)
- BNC male to BNC male, 75 Ω cable from ITT Pomona Electronics (part number 2249-E-xx)
- BNC female to RCA phono plug adapter, from ITT Pomona Electronics (part number 5319)
- BNC 50 Ω feed-through terminator adapter from ITT Pomona Electronics (part number 4119-50)
- BNC female-female adapter from ITT Pomona Electronics (part number 3283)

C

Frequency Resolution and Lookup Memory in DDS Mode

For DDS-based waveform generation, you must first load one cycle of the desired waveform into the lookup memory. The size of the DDS lookup memory is 16,384 samples. Each sample is 16 bits wide.

Note One cycle of the waveform buffer loaded into the memory should be exactly equal to the size of the DDS lookup memory.

F_c = update clock for the accumulator.

Set the NI 5411/5431 at F_c = 40 MHz.

F_a = desired frequency of the output signal

N = accumulator size in bits

Set the NI 5411/5431 at N = 32.

FCW = frequency control word to be loaded into the accumulator to generate F_a.

The frequency control word is calculated using the formula:

$FCW = (2^N * F_a) / F_c$

The frequency resolution is then given by:

frequency resolution = $F_c / 2^N = (40 \times 10^6) / 2^{32} = 9.31322$ mHz

For example, if you need to generate a frequency of 10 MHz, then the FCW is (2^{32} * 10E6)/40E6, which equals 1,073,741,824. If you need to generate a frequency of 1 Hz, then the FCW is (2^{32} * 1)/40E6, which equals 107.

Note On the NI 5411, the maximum frequency of a sine wave you can generate reliably is limited to 16 MHz and, for the NI 5431, it is limited to 8 MHz.. Other waveforms such as square or triangular waves are limited to 1 MHz.

You can also synthesize arbitrary waveforms using DDS. Generating arbitrary waveforms this way will be very limited; you are restricted to a single buffer, and this buffer should be exactly equal to the size of the lookup memory (16,384 samples).

To update every sample of an arbitrary waveform in lookup memory at the maximum clock rate of 40 MHz, the software writes an FCW value of $2^{(N-L)}$, where N is the size of the accumulator and L is the number of address bits of lookup memory (L = 14 bits). Thus, the FCW value for the NI 5411/5431 equals 262,144. Since FCW = $(2^N * F_a) / F_c$, $F_a = (2^{(N-L)} * F_c) / 2^N$, so you would write a frequency value of $(2^{(32-14)} \times (40 \times 10^6)) / 2^{32}$, which equals 2.441 kHz

If you want to update every sample in lookup memory at an integral subdivision, D, of the maximum clock rate, then you want an FCW value of $2^{(N-L-D+1)}$. In other words, for an effective update rate of every sample at half the maximum clock rate, write a frequency value of $(2^{(32-14-2+1)} \times (40 \times 10^6)) / 2^{32}$, which equals 1.221 kHz.

D

Technical Support Resources

This appendix describes the comprehensive resources available to you in the Technical Support section of the National Instruments Web site and provides technical support telephone numbers for you to use if you have trouble connecting to our Web site or if you do not have internet access.

NI Web Support

To provide you with immediate answers and solutions 24 hours a day, 365 days a year, National Instruments maintains extensive online technical support resources. They are available to you at no cost, are updated daily, and can be found in the Technical Support section of our Web site at `www.natinst.com/support`.

On-Line Problem-Solving and Diagnostic Resources

- **KnowledgeBase**—A searchable database containing thousands of frequently asked questions (FAQs) and their corresponding answers or solutions, including special sections devoted to our newest products. The database is updated daily in response to new customer experiences and feedback.
- **Troubleshooting Wizards**—Step-by-step guides lead you through common problems and answer questions about our entire product line. Wizards include screen shots that illustrate the steps being described and provide detailed information ranging from simple getting started instructions to advanced topics.
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Software-Related Resources

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Glossary

Prefix	Meaning	Value
μ-	micro-	10^{-6}
m-	milli-	10^{-3}
k-	kilo-	10^{3}
M-	mega-	10^{6}

Numbers/Symbols

%	percent
+	positive of, or plus
–	negative of, or minus
±	plus or minus
/	per
°	degree
Ω	ohm
+5 V	+5 V output signal

A

A	amperes
amplification	method of scaling the signal level to a higher level
ARB	normal waveform output signal
Arb mode	a mode of generating waveforms in which waveforms are defined by multiple buffers that can be linked or looped in any order

arbitrary waveform generator	instrument for generating any desired waveform; this instrument is not restricted to standard waveforms such as sine or square
attenuation	decreasing the amplitude of a signal

B

b	bit—one binary digit, either 0 or 1
B	byte—eight related bits of data, an eight-bit binary number. Also used to denote the amount of memory required to store one byte of data.
BNC	a type of coaxial signal connector
buffer	temporary storage for acquired or generated data
burst trigger mode	repeats a stage until a trigger advances the waveform to the next stage
bus	the group of conductors that interconnect individual circuitry in a computer. Typically, a bus is the expansion vehicle to which I/O or other devices are connected. Examples of PC buses are the AT bus (also known as the ISA bus) and the PCI bus.

C

C	Celsius
CalDAC	calibration DAC
clock	hardware component that controls timing for reading from or writing to groups
CMOS	complementary metal-oxide semiconductor
continuous trigger mode	repeats a staging list until waveform generation is stopped
counter	a circuit that counts external pulses or clock pulses (timing)
coupling	the manner in which a signal is connected from one location to another

D

DAC	digital-to-analog converter—an electronic device, often an integrated circuit, that converts a digital number into a corresponding analog voltage or current
dB	decibel—the unit for expressing a logarithmic measure of the ratio of two signal levels: dB = 20 log 10 V1/V2, for signals in volts
dBc	decibel referred to carrier level
DC	direct current
DC coupled	allowing the transmission of both AC and DC signals
DDS	direct digital synthesis—a digital technique of frequency generation using a numerically controlled oscillator (NCO), a dedicated lookup memory, and a DAC
DDS mode	a method of waveform generation that uses built-in DDS functionality to generate very high frequency resolution standard waveforms
DGND	digital ground signal
digital word	*See* word.
driver	software that controls a specific hardware device
DUT	device under test
dynamic range	the ratio of the largest signal level a circuit can handle to the smallest signal level it can handle (usually taken to be the noise level), normally expressed in dB

E

EEPROM	electrically erasable programmable read-only memory—ROM that can be erased with an electrical signal and reprogrammed
external trigger	a voltage pulse from an external source that triggers an event such as A/D conversion
EXT_TRIG	external trigger input signal

F

FIFO	first-in first-out memory buffer—the first data stored is the first data sent to the acceptor. FIFOs are often used on DAQ devices to temporarily store incoming or outgoing data until that data can be retrieved or output. For example, an analog input FIFO stores the results of A/D conversions until the data can be retrieved into system memory, a process that requires the servicing of interrupts and often the programming of the DMA controller. This process can take several milliseconds in some cases. During this time, data accumulates in the FIFO for future retrieval. With a larger FIFO, longer latencies can be tolerated. In the case of analog output, a FIFO permits faster update rates, because the waveform data can be stored on the FIFO ahead of time. This again reduces the effect of latencies associated with getting the data from system memory to the DAQ device.
filters	digital or analog circuits that change the frequency characteristics of a waveform
frequency hop	change from one frequency to another
frequency resolution	the smallest frequency change that can be generated by a NI 5411/5431
frequency sweep	change the frequency of a waveform in a controlled manner

G

gain	the factor by which a signal is amplified, sometimes expressed in decibels
GUI	graphical user interface

H

hardware	the physical components of a computer system, such as the circuit boards, plug-in boards, chassis, enclosures, peripherals, cables, and so on
high-resolution clocking mode	a method of waveform generation in which the update clock frequency is set to any value from 0 to 40 MHz with a resolution of approximately 40 mHz
HiZ	high impedance
Hz	hertz—the number of cycles or repetitions per second

I

I/O	input/output—the transfer of data to/from a computer system involving communications channels, operator interface devices, and/or data acquisition and control interfaces
IFIFO	instruction FIFO
instruction FIFO	the FIFO that stores the waveform generation staging list
ISA	industry standard architecture

K

k	kilo—the standard metric prefix for 1,000, or 10^3, used with units of measure such as volts, hertz, and meters
K	kilo—the prefix for 1,024, or 2^{10}, used with B in quantifying data or computer memory
kS	1,000 samples
Kword	1,024 words of memory

L

latch	a digital device that stores digital data based on a control signal
level DAC	the calibration DAC used to change the voltage levels to another device
linking	linking different buffers stored in the waveform memory
looping	repeating the same buffer in the waveform memory. This method of waveform generation decreases memory requirements.
lowpass filter	a circuit used to smooth the waveform output and removed unwanted high frequency contents form the signal

M

m	meters
M	(1) Mega, the standard metric prefix for 1 million or 10^6, when used with units of measure such as volts and hertz; (2) mega, the prefix for 1,048,576, or 2^{20}, when used with B to quantify data or computer memory
marker	a digital signal that is generated on a pin on the digital I/O connector at a requested point in the waveform buffer; this happens while the analog waveform is being generated at the NI 5411 Arb output connector
MARKER	marker output signal
marker offset	the position, in number of samples, from the start of the waveform buffer at which the marker is requested
master/slave	locking the NI 5411/5431 clock in frequency and phase to an external phase locking reference clock source
MB	megabytes of memory

N

noise	an undesirable electrical signal—Noise comes from external sources such as the AC power line, motors, generators, transformers, fluorescent lights, soldering irons, CRT displays, computers, electrical storms, welders, radio transmitters, and internal sources such as semiconductors, resistors, and capacitors. Noise corrupts signals you are trying to send or receive.
NTSC	video standard in North America and Japan

O

output enable relay	a relay switch at the output of the NI 5411 that can enable the waveform generation at any time or that can connect the output to ground

P

PA<0..15>	digital pattern generator outputs

PAL	video standard in some European and Asian countries
passband	the range of frequencies which a device can properly propagate or measure
pattern generation	a type of handshaked (latched) digital I/O in which internal counters generate the handshaked signal, which in turn initiates a digital transfer. Because counters output digital pulses at a constant rate, this means you can generate and retrieve patterns at a constant rate because the handshaked signal is produced at a constant rate.
PCI	Peripheral Component Interconnect—a high-performance expansion bus architecture originally developed by Intel to replace ISA and EISA. It is achieving widespread acceptance as a standard for PCs and work-stations; it offers a theoretical maximum transfer rate of 132 Mbytes/s.
PCLK	digital pattern clock output
peak-to-peak	a measure of signal amplitude; the difference between the highest and lowest excursions of the signal
pipeline	a high-performance processor structure in which the completion of an instruction is broken into its elements so that several elements can be processed simultaneously from different instructions
PLL	phase-locked loop—a circuit that synthesizes a signal whose frequency is exactly proportional to the frequency of a reference signal
PLL Ref	a PLL input that accepts an external reference clock signal and phase locks to it the NI 5411 internal clock
Plug and Play devices	devices that do not require dip switches or jumpers to configure resources on the devices—also called switchless devices
ppm	parts per million
pre-attenuation offset	an offset provided to the signal before it reaches the attenuators
protocol	the exact sequence of bits, characters, and control codes used to transfer data between computers and peripherals through a communications channel, such as the GPIB bus
PXI	PCI eXtensions for Instrumentation

R

resolution	the smallest signal increment that can be detected by a measurement system. Resolution can be expressed in bits, in proportions, or in percent of full scale. For example, a system has 12-bit resolution, one part in 4,096 resolution, and 0.0244 percent of full scale.
RTSI bus	Real-Time System Integration bus—the National Instruments timing bus that connects DAQ boards directly, by means of connectors on top of the boards, for precise synchronization of functions

S

s	seconds
S	samples
sampling rate	the rate, in samples per second (S/s), at which each sample in the waveform buffer is updated
SCSI	Small Computer System Interface (bus)
sequence list	*See* staging list.
shift-keying	frequency shift keying (FSK)
single trigger mode	when the arbitrary waveform generator goes through the staging list only once
SMB	Sub Miniature Type B connector that features a snap coupling for fast connection
S/s	samples per second—used to express the rate at which a DAQ board samples an analog signal
stage	in Arb mode, specifies the buffer to be generated, the number of loops on that buffer, the marker position for that buffer, and the sample count for the buffer; for DDS mode, specifies the frequency to be generated of the waveform in the lookup memory and the time for which that frequency has to be generated
staging list	a buffer that contains linking and looping information for multiple waveforms; also known as a sequence list or waveform sequence

stepped trigger mode	a mode of waveform generation used when you want a trigger to advance the waveforms specified by the stages in the staging list
SYNC	TTL version of the sine waveform output signal generated by the NI 5411/5431

T

trigger	any event that causes or starts some form of data capture
TTL	transistor-transistor logic

U

update rate	the rate at which a DAC is updated

V

V	volts
VCXO	voltage controlled crystal oscillator
VHDSCSI	very high-density SCSI

W

waveform	multiple voltage readings taken at a specific sampling rate
waveform buffer	the collection of 16-bit data samples stored in the waveform memory that represent a desired waveform. Also known as a waveform segment.
waveform linking and looping	*See* linking, looping.
waveform memory	physical data storage on the NI 5411/5431 for storing the waveform data samples
waveform segment	*See* waveform buffer.

waveform sequence	*See* staging list.
waveform staging	*See* linking, looping.
word	The standard number of bits that a processor or memory manipulates at one time. Microprocessors typically use 8-, 16-, or 32-bit words.

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Numbers

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